SMJ1209

2 Form C

100V / 750mA

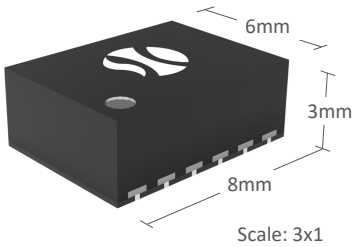
MOSFET Output Solid State Relay

Package

12DFN (8x6x3mm)

Actual Size





Scale: 3x1

Description

The SMJ1209 is a 2 Form C relay that offers a high reliability alternative to EMRs in Semiconductor test applications.

Packaged in a miniature 12DFN (8x6mm) outline, the SMJ1209 uses less board space than alternative discrete SSR designs.

Guaranteed break-before-make operation further offers easier implementation than designs using discrete SSRs and additional control circuitry. No external timing circuits are required to achieve correct switch Open-Close Gap timing.

Applications

- Electro-Mechanical Relay (EMR) Replacement
- Automatic Test Equipment
- High Volume Semiconductor Test
- Data Acquisition
- Medical Equipment
- Battery Monitoring
- Safety Systems
- Inverting/Summing Amplifiers (T-Switch)

Features

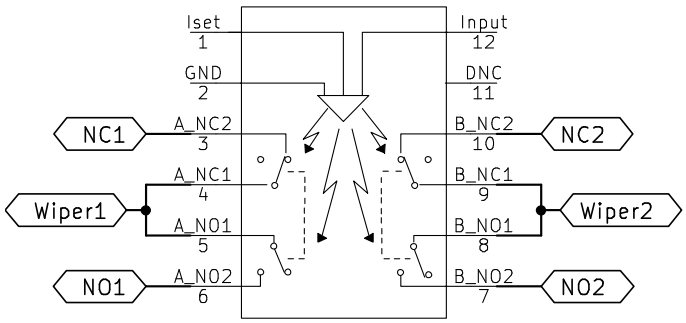
- Ultra-Compact 8x6mm DFN Package
- True 2 Form C Break-Before-Make Switch Operation
- Low On Resistance (500mΩ TYP)
- Low Output Capacitance (18pF TYP @ 25V)
- High voltage (100V) suitable for many automotive component test requirements
- Low Output Leakage (1nA MAX @ 80V, <100pA @10V,<1pA in T-Switch configuration)
- 750mA Maximum Continuous Load Current
- 2A Pulsed Current (100ms Period @ 10% Duty Cycle)
- $V_{IN(low)}$ of 1.1V - suitable with Darlington or Open Collector
- Isolation Voltage (300VRMS)
- Long Life / High Reliability

Advantages over Electro-Mechanical Relays (EMRs)

- 1 Billion+ Switch Actuations Operating Life
- Bounce Free Switching
- On Resistance Low and Stable over time and actuations
- Third State “All Switches Open” available to enable specific DUT site isolation during multi-site ATE testing
- Wide Operational Voltage Range (4.5V—16.0V), one part number can replace broad spectrum of EMR devices
- No Magnetic Interference with closely spaced devices
- No Dissimilar Metal Thermal EMF generated across contacts
- T-Switch Connectivity Option (ultra low leakage)

Schematic / Functional Diagram

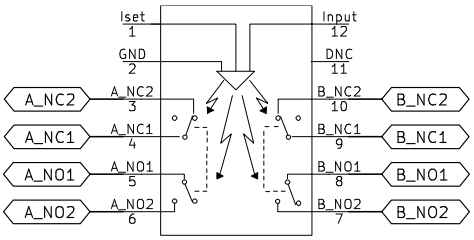
Classic 2 Form C (DPDT)



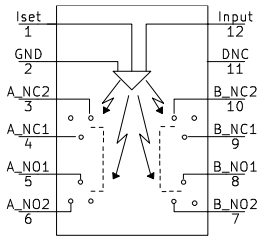
Sample Applications

Figure 1: *Additional Schematic / Functional Connection Diagrams*

Ganged 2 Form A / 2 Form B (4PST)



All Switches Open (Test Site Isolation)



T-Switch (I/O Signal Isolation)

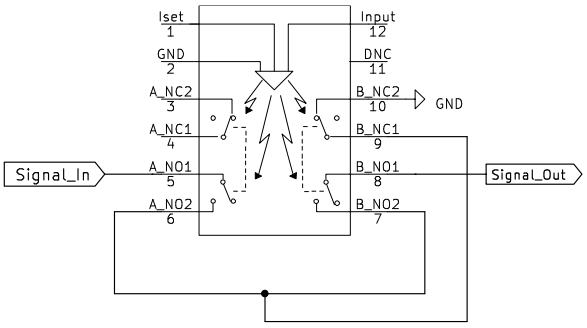
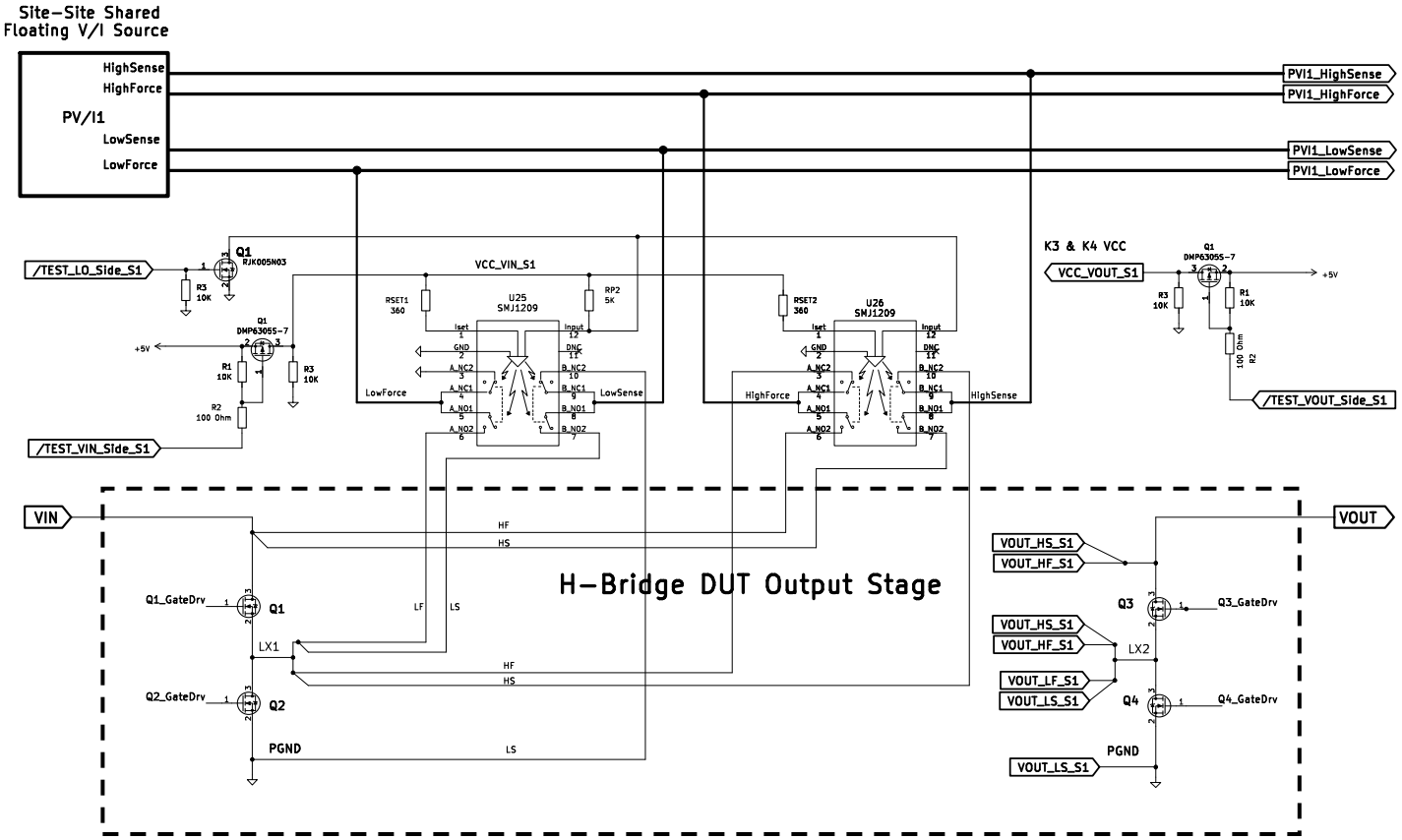


Figure 2: *H-Bridge High Side - Low Side FETs RON Test with Shared Floating V/I*
Dual Form C DPDT for Kelvin Force - Sense Switching : Grounded and Floating Loads



Absolute Maximum Ratings

The values indicated are absolute stress ratings. Functional operation of the device is not implied at these or any conditions in excess of those defined in the electrical characteristics section of this document. Exposure to absolute Maximum Ratings may cause permanent damage to the device and may adversely affect reliability.

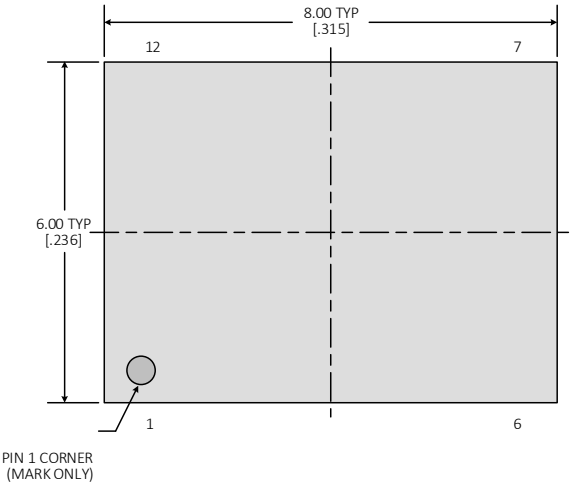
Storage Temperature	-55 to +125°C
Operating Temperature	-40 to +85°C
Continuous Input Current	50mA
Transient Input Current	500mA
Input Power Dissipation	40mW
Output Power Dissipation	600mW
Solder Temperature – Wave (10s)	260°C
Solder Temperature – IR Reflow (10s)	260°C
Input Control Voltage	-0.5V - 16V
Total Supply Voltage (VCC to GND)	18.0V
INPUT Pin Voltage	18.0V to (GND-0.3V)
NC1 to NC2 Blocking Voltage	±105V
NO1 to NO2 Blocking Voltage	±105V
Control to Switch Isolation Voltage	$315V_{RMS}$

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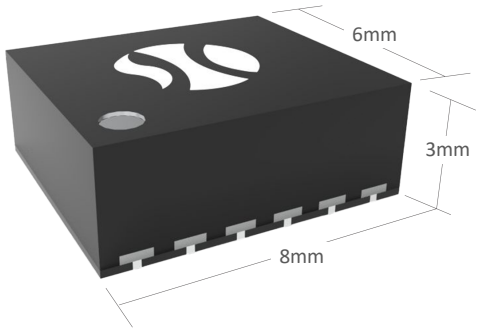
Package Dimensions

NOTE: Dimensions in mm (in)

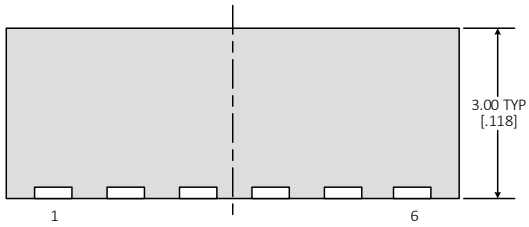
Top View



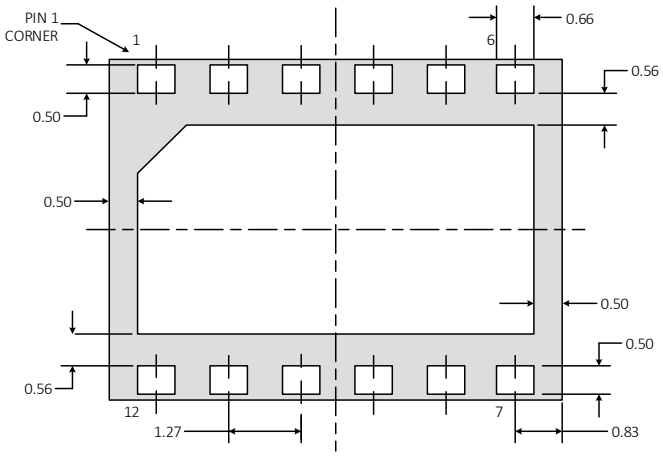
ISO View



Side View



Bottom View



Notes:

- Drawings are not to scale
- All dimensions are in millimeters
- Dimensions of Exposed Pad on bottom of package do not include Mold Flash
- Mold Flash, if present, shall not exceed 0.15mm on any side

Electrical Characteristics, T_A = 25°C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Specifications						
Control Voltage Operational Range[1]	V_{CC}	4.5	-	16	V	-
Input Control Low Level[1]	$V_{IN(Low)}$	-	-	1.1	V	-
Input Control Low Level Current	$I_{IN(Low)}$	4	I_{SET}	12	mA	$V_{IN(Low)}$ = 0.8V
Input Control High Level[1]	$V_{IN(High)}$	-	Pull-up to V_{CC}	-	V	-
Input Control High Level Current	$I_{IN(High)}$	-	-	400	µA	V_{IN} = 16V
Control Current[2]	I_{SET}	4	8	12	mA	Guaranteed Break-Before-Make
Control Voltage[3] (Optical Control Circuit)	V_{SET}	2.0	2.15	2.4	V	I_{SET} = 8mA
V_{IN} Driver Transition Time[4]	T_R & T_F	-	-	5	µs	-
Output Specifications (Same for both NO and NC poles)						
Blocking Voltage	V_B	100	-	-	V	-
Continuous Load Current	I_O	-	-	750	mA	-
Maximum Pulsed Current	$I_{O(Pulse)}$			2	A	Period = 100ms @ 10% Duty Cycle
On Resistance	R_{ON}	-	500	750	mΩ	I_O=750mA
Open Switch Leakage Current	I_{Oleak}	-	-	100	nA	V_O=100V
		-	-	1		V_O=80V
		-	100	-	pA	V_O=10V
Open Switch Capacitance Between Terminals	C_{OUT}	-	75	-	pF	V_O=0, f=1MHz
		-	18	-		V_O=25, f=1MHz
		-	12	-		V_O=60, f=1MHz

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Electrical Characteristics, cont'd, T_A = 25°C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Coupled Specifications						
Turn-On Time	T_{ON}	-	1500	6000	µs	I_{SET} = 3mA, I_O = 400mA
		-	1000	3000		I_{SET} = 4mA, I_O = 400mA
		-	600	1500		I_{SET} = 8mA, I_O = 400mA
		-	400	1000		I_{SET} = 12mA, I_O = 400mA
Turn-Off Time	T_{OFF}	-	50	-	µs	-
Break-before-Make Gap Time[5]	T_{GAP}	700	1300	-	µs	I_{SET} = 3mA, I_O = 400mA
		400	900	-		I_{SET} = 4mA, I_O = 400mA
		200	400	-		I_{SET} = 8mA, I_O = 400mA
		100	250	-		I_{SET} = 12mA, I_O = 400mA
Input to Output Capacitance	C_S	-	0.6	-	pF	V=0, f=1MHz
Contact Transient Ratio	-	2,000	7,000	0	V/µs	dV = 50V
Isolation Specifications						
Isolation Voltage	V_{ISO}	300	-	-	V_{RMS}	RH ≤ 50%, t=1min
Input-Output Resistance	R_{I-O}	-	10^{12}	-	W	VI-O = 500V_{DC}

Notes:

1. Input Control High Level is controlled by the pull-up resistor (R_P) to V_{CC}. For more details, reference the Connection Diagram found in Figure 20 on page 11
2. Control Current is referred to as "I_{SET}" in the Connection Diagram found in Figure 20 on page 11. See Note 5 on page 11 as well for more details. Switches will operate with Break-Before-Make timing with I_{SET} currents as low as 3mA, however T_{ON} and T_{GAP} will have longer delay times. Please see graphs in Figures 10 - 13 on page 8 for typical delay times with various (from "lower") I_{SET} values
3. V_{SET} is discussed in the Connection Diagram Section found on page 11. V_{SET} is referenced in Note 5 as "Vopticalcircuit" and is used therein to show calculations for R_{SET} values. V_{SET} relation to I_{SET} can be found in Figure 9 on page 8
4. Rise / Fall time of INPUT control signal
5. Break-Before-Make time refers to the time "gap" between the Normally Closed Turn Off Time and the corresponding Normally Open portion's Turn On Time. Figure 13 on page 8 shows typical values versus I_{SET} while also giving expected gap times at low and high temperature operation

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Performance Characteristics Plots, T_A = 25°C (unless otherwise specified)

Figure 3: *Typical Turn-On Time Distribution (N=100)*

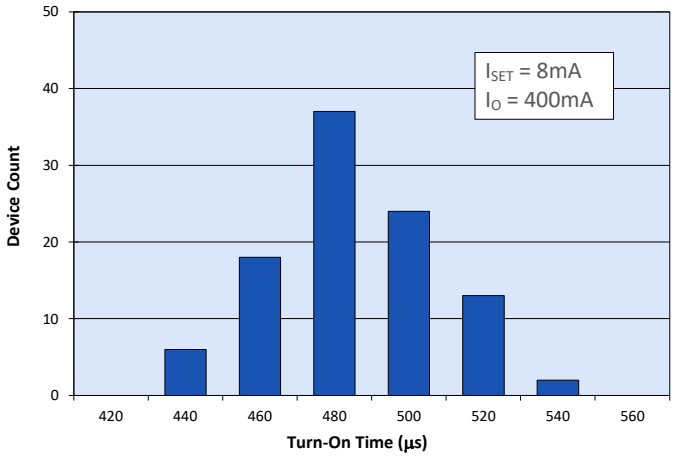


Figure 4: *Typical Turn-Off Time Distribution (N=100)*

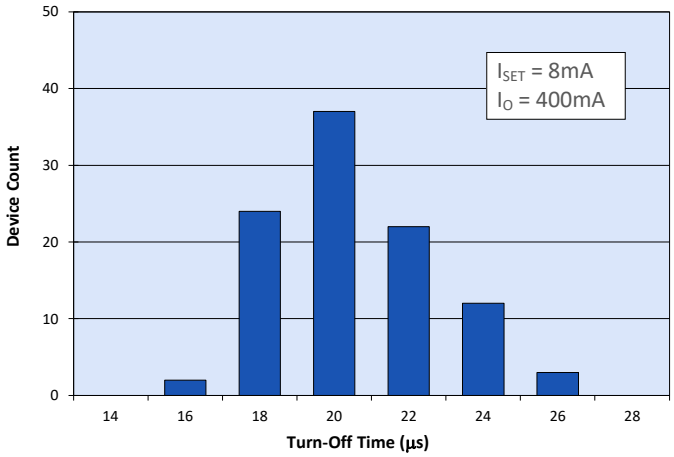


Figure 5: *Typical On Resistance Distribution (N=100)*

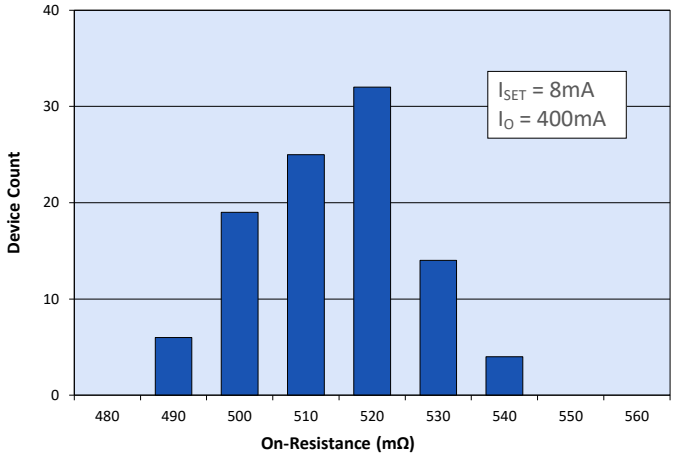


Figure 6: *Typical Blocking Voltage Distribution (N=100)*

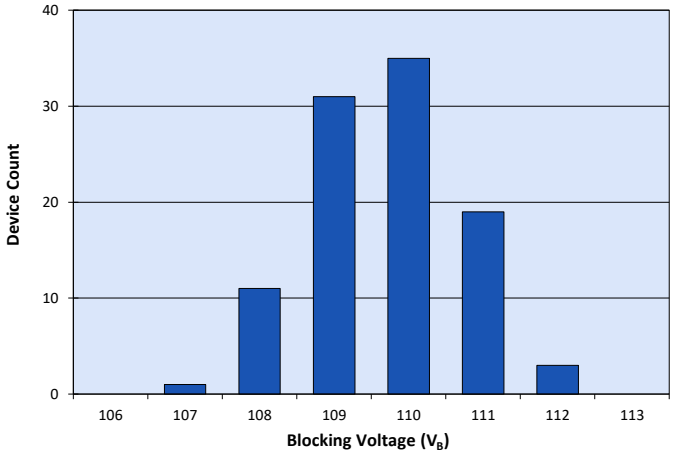


Figure 7: *Typical Output Leakage vs. Voltage*

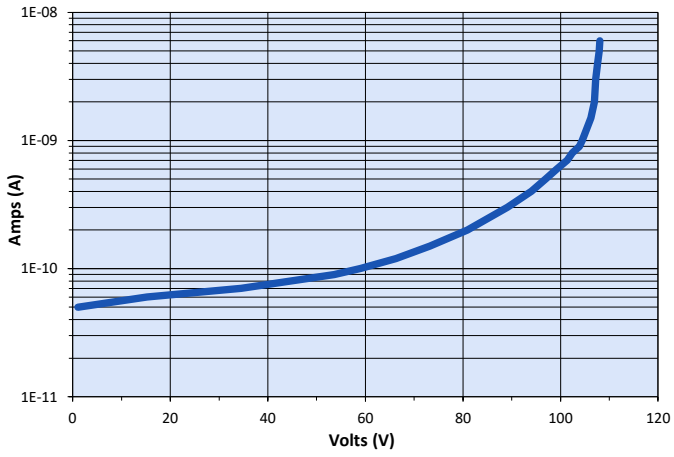
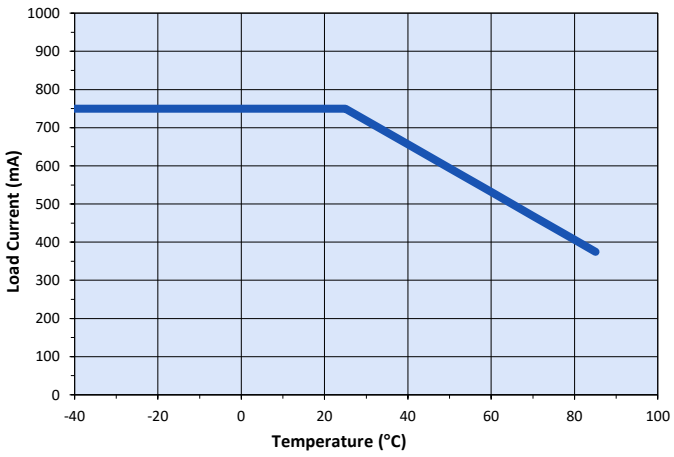


Figure 8: *Maximum Load Current vs. Temperature*



Performance Characteristics Plots, cont'd, T_A = 25°C (unless otherwise specified)

Figure 9: *V_{SET} vs. I_{SET}*

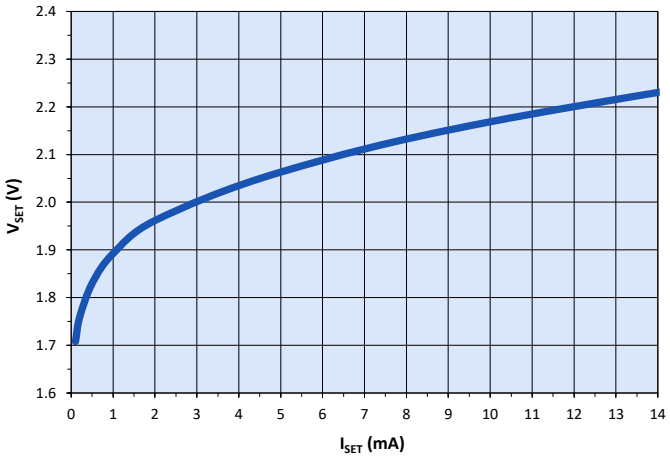


Figure 10: *Turn-On Time vs. I_{SET}*

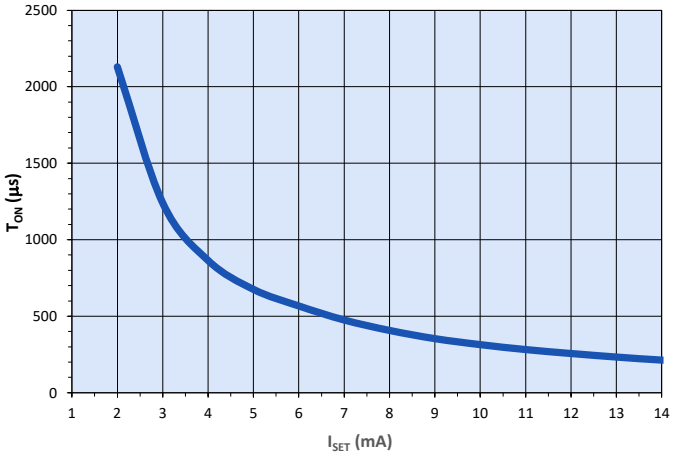


Figure 11: *Turn-On Time vs. I_{SET} (Time Scale zoomed for detail)*

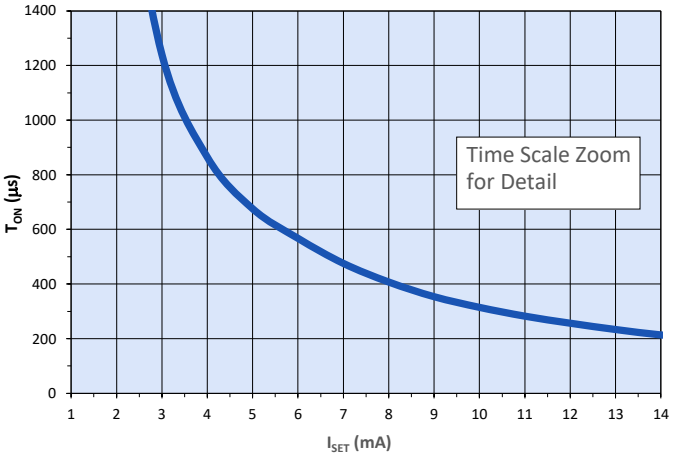


Figure 12: *Turn-Off Time vs. I_{SET}*

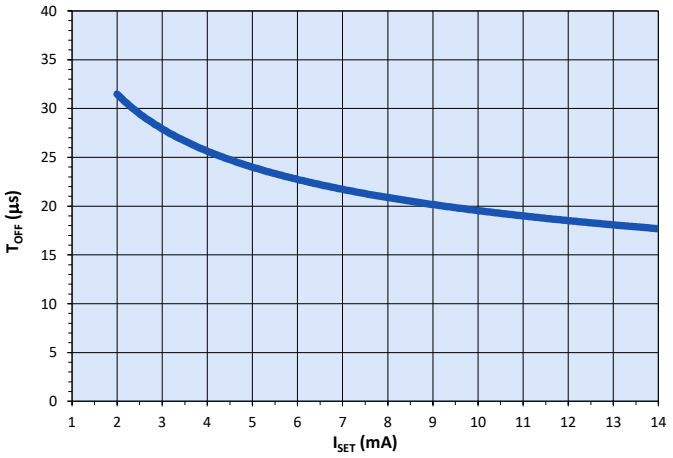
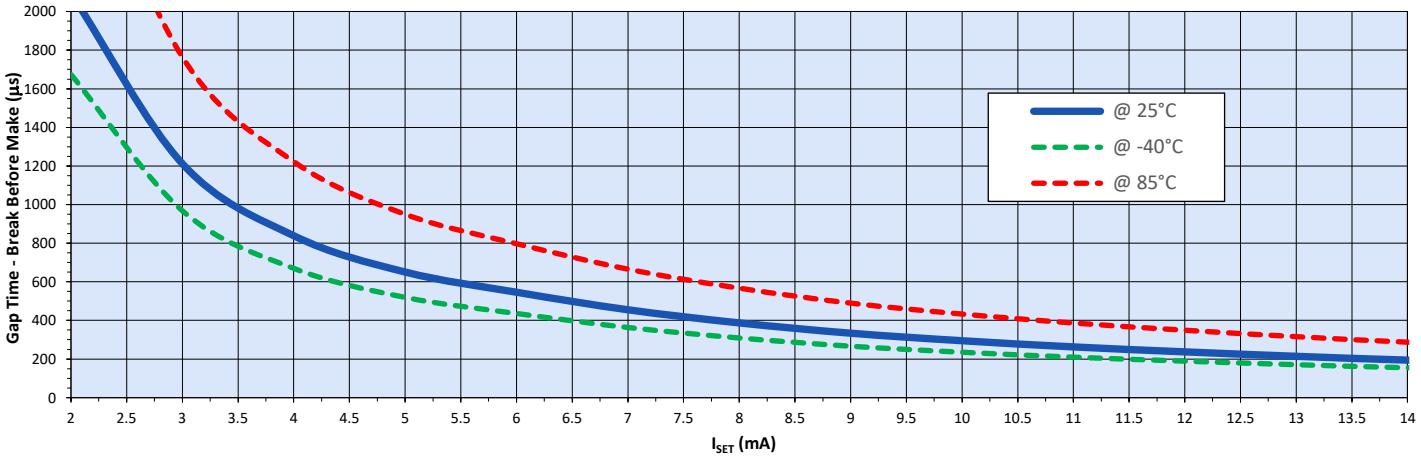


Figure 13: *Typical Gap Time vs. I_{SET} (I_{SET} value @ 25°C)*



Performance Characteristics Plots, cont'd, T_A = 25°C (unless otherwise specified)

Figure 14: *Normalized Typical I_{SET} vs. Temperature*

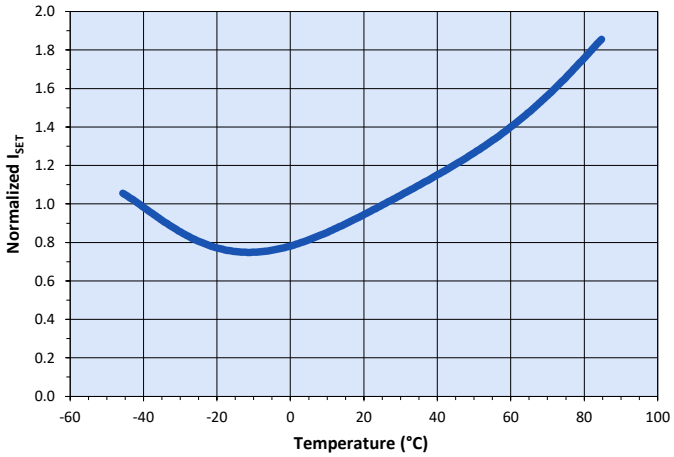


Figure 15: *Normalized Typical V_{SET} vs. Temperature*

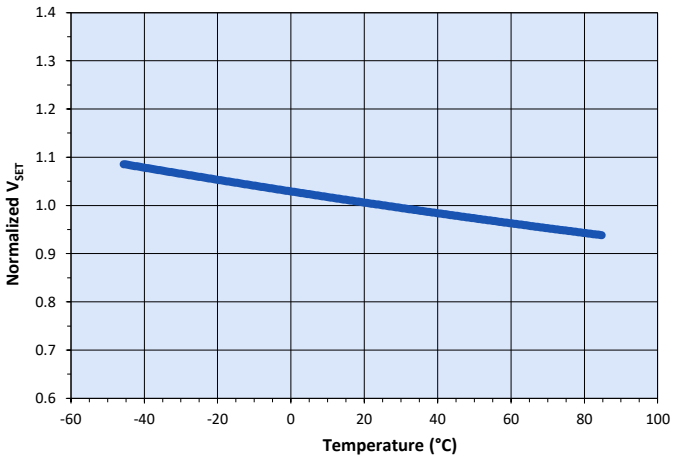


Figure 16: *Normalized Typical Turn On Time vs. Temperature*

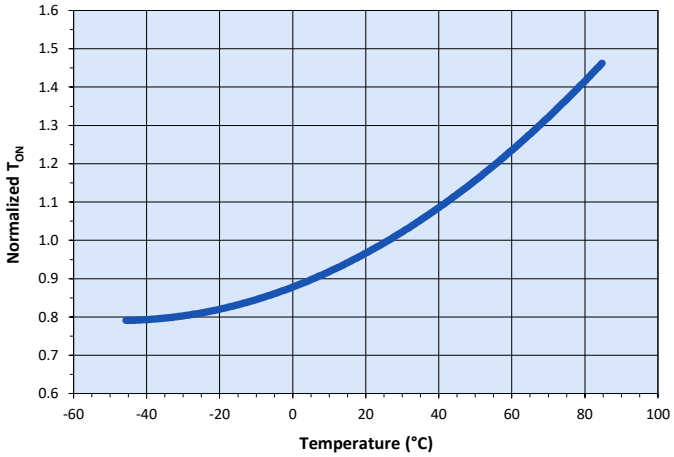


Figure 17: *Normalized Typical Turn Off Time vs. Temperature*

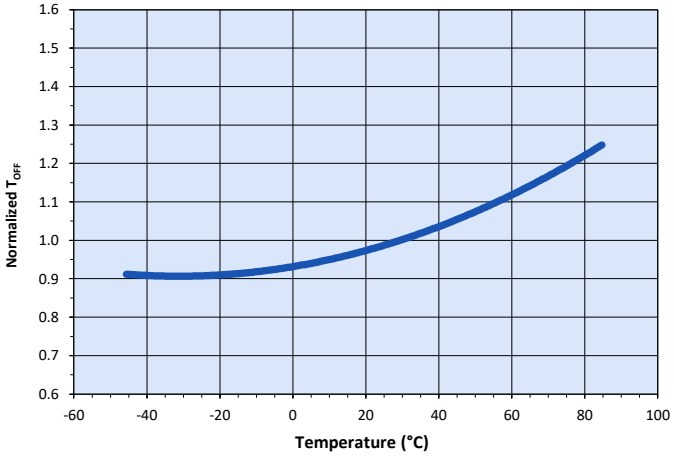


Figure 18: *Normalized Typical R_{ON} vs. Temperature*

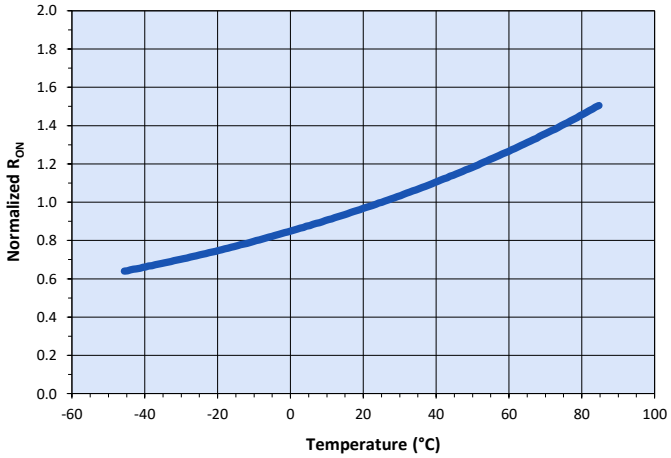
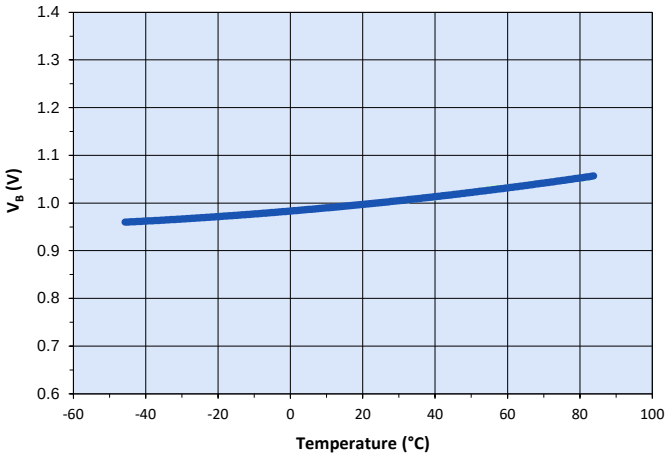


Figure 19: *Normalized Typical V_B vs. Temperature*



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Pin Functions / Definitions / Identification

ISET: Input to Optical Control and Timing circuit. ISET pin has a nominal 2.15V voltage drop @ ISET=8mA when pulled up to V_{CC} through RSET current setting resistor. This 2.15V drop needs to be subtracted from V_{CC} when computing ISET value:
ISET= (V_{CC} — 2.15)/RSET
ISET flows continuously when SMJ1209 device is powered up. ISET returns through GND pin when Input=VCC. ISET current returns through INPUT pin to Relay Driver Output stage to System Ground when INPUT < VIN(Low) level

DNC: Do Not Connect. Factory use only, Do not connect to any trace on PCB

GND: SMJ1209 Ground pin. Should be terminated to the system Logic Control ground reference. ISET flows (returns) through GND pin when INPUT pin is pulled up to Vcc

INPUT: Operational Control input for SMJ1209 device. Must be pulled up to VCC through 10K Ohm or lower resistor

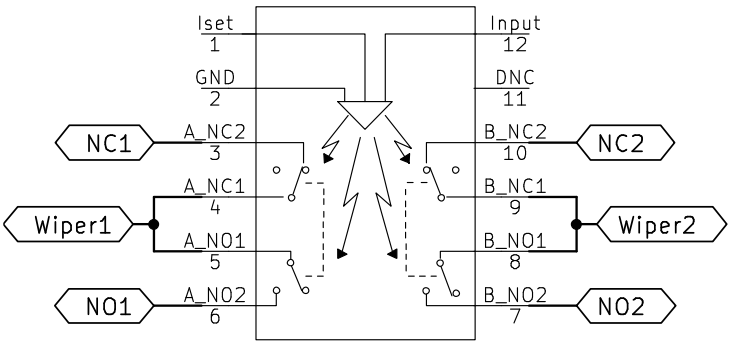
- Voltage Level sensitive: when INPUT pin is pulled up to Vcc through Rp resistor, the Normally Closed switch pair contacts (A_NC1, A_NC2 and B_NC1, B_NC2) are closed, contact resistance = RON. Normally Open switch pair contacts (A_NO1, A_NO2 and B_NO1, B_NO2) are high resistance, contact resistance @ 80V blocking voltage = 80V/1nA = 80GΩ. This state corresponds to “Idle” non-activated functional state for EMR relays
- When INPUT is pulled below VIN(Low) Threshold 1.1V, the NO-NC switch pair contacts reverse states. Timing of NC switch pair opening, and NO switch pair closing is controlled by internal Break-Before-Make timing circuits. Break-Before-Make timing control remains in effect when switches are returning to idle state condition

A_NO1, A_N02, B_NO1, B_NO2: Normally Open switch contacts (Form A type) when INPUT pulled up to Vcc. The switch contacts can carry bi-directional current flow, not polarity sensitive. The NO1, NO2 pin pairs go to low resistance, Ron, when INPUT is pulled below VIN (Low) threshold. Externally connect A_NC1 to A_NO1 (and likewise B_NC1 to B_NO1) to achieve 2 Form C Double Pole Double Throw (DPDT) switch function, controlled by INPUT threshold level

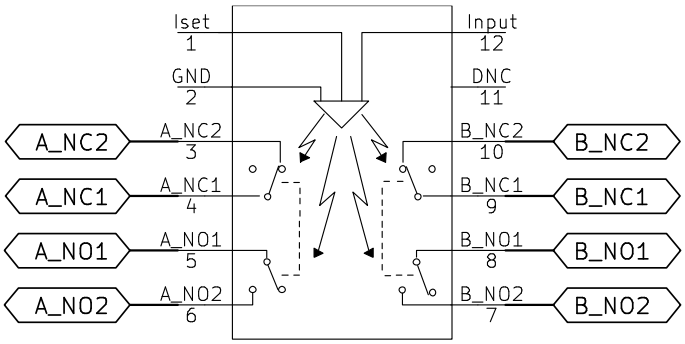
A_NC1, A_NC2, B_NC1, B_NC2: Normally Closed switch contacts (Form B type) when INPUT pulled up to Vcc. The switch contacts can carry bi-directional current flow, not polarity sensitive. The NC1, NC2 pin pairs go to high resistance, Low Leakage, IO(Leak), when INPUT is pulled below VIN(Low) threshold. Externally connect A_NC1 to A_NO1 (and likewise B_NC1 to B_NO1) to achieve 2 Form C DPDT switch function. If NC1 pairs are not externally connected to NO1 pairs, then NC switch pairs and NO switch pairs can be connected to independent signals, and the switches Open-Close functionality will be ganged in operation to INPUT pin threshold level, achieving Double Pole, Double Throw functionality (DPDT)

Exposed Pad: Exposed Pad on underside of package is not electrically connected to any internal circuits. The Exposed Pad can be left unconnected electrically or be connected to quiet (Analog / Signal) Ground reference on PCB. Connecting to quiet Ground reference point will reduce parasitic capacitive coupling between Control side of device and Switch contacts through the Exposed Pad.

2 Form C
DPDT - Functional Diagram

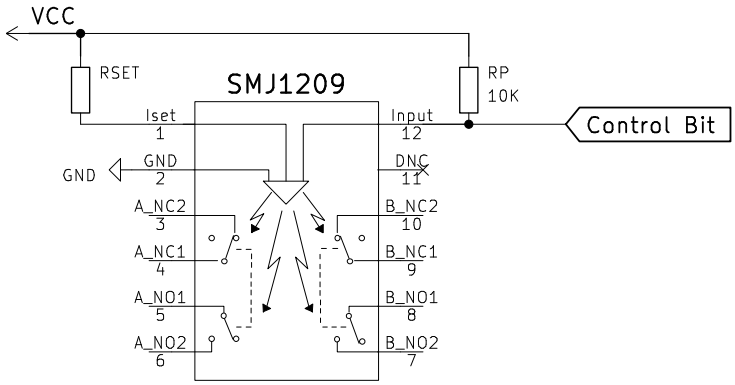


Ganged 2 Form A / 2 Form B
4PST - Functional Diagram



Recommended Connections and Components

Figure 20: SMJ1209 Connection Diagram



1. SSO recommends a Pull Up Resistor (Rp) value of 10kΩ or less to Vcc
2. NO (Normally Open) contacts between pins 5 & 6 (Channel A) and between pins 7 & 8 (Channel B) are defined as OPEN when the Open Collector is open and pin 12 is pulled up with the Pull Up Resistor (Rp) to Vcc. These contacts will CLOSE when the Open Collector driver pulls pin 12 below $V_{IN(LOW)}$. The NC (Normally Closed) contacts between pins 3 & 4 (Channel A) and between pins 9 & 10 (Channel B) operate in an inverse manner. For more information, refer to the section discussing Operational Logic Truth on page 12
3. $V_{IN(LOW)}$ Max specification of 1.1V enables the SMJ1209 Input Control Logic to be backward compatible with legacy EMR relay drivers with Darling Output stages. User should verify that $V_{CE(SAT)}$ specifications of target system meets this 1.1V threshold requirement
4. The Open Collector Transition Time (Tr and Tf) should be less than 5µs for proper functional operation
5. Iset (Control Current as found in Parameters on Page 5) is used to set the internal photo drive current. SSO recommends an Iset value of 8mA for optimal device performance. Rset can be calculated for Vcc of 4.5V to 16.0V. Assume a voltage drop (V_{SET}) of 2.15V for the Optical Control Circuit and Rset values for a 8mA Iset become:

   Rset (@$5V_{CC}$) = (Vcc-Vset) / (target Iset) = (5V-2.15V) / (0.008A) = 2.85 / 0.008 (356 ohms)

   Rset (@12Vcc) = (Vcc-Vset) / (target Iset) = (12V-2.15V) / (0.008A) = 9.85 / 0.008 (1230 ohms)

   Rset (@5Vcc) = 360 Ohm (5%) **Rset (@12Vcc) = 1200 ohms (5%)**

   Above calculations are for power supplies with acceptable tolerances of ±10%. If tolerances go beyond this range, calculate Rset values based on the lowest voltage in the tolerance range
6. Iset can be programmed to over an operational range of 3mA to 12mA with guaranteed Break-Before-Make switch operation. Lower values of Iset will cause the device to have slower Ton and wider Tgap times, higher values of Iset will result in faster Ton and narrower Tgap times. This allows the user to optimize device power consumption vs switching speed per end application requirements. Please see Electrical Characteristics Table and Figures 10-13 on page 8 for more information
7. The same Vcc value should be used for both Rset (as calculated above) and the pull-up resistor (Rp) used with Vin (pin 12) discussed in note 1 above
8. Pins 4 & 5 (Channel A) and Pins 8 & 9 (Channel B) as shown in Figure 20 can be connected externally forming a common point, in effect the common point (wiper) of the Form C relay. If these pins are not connected externally, the NO and NC switches can be connected to independent signals or loads, with open-close functionality ganged by Control Circuit. See Figure 1 on page 2, “Ganged 2 Form A / 2 Form B (4PST)” as an example

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Dual Form C Operational Truth Table

Figure 21: Basic Functional Circuit

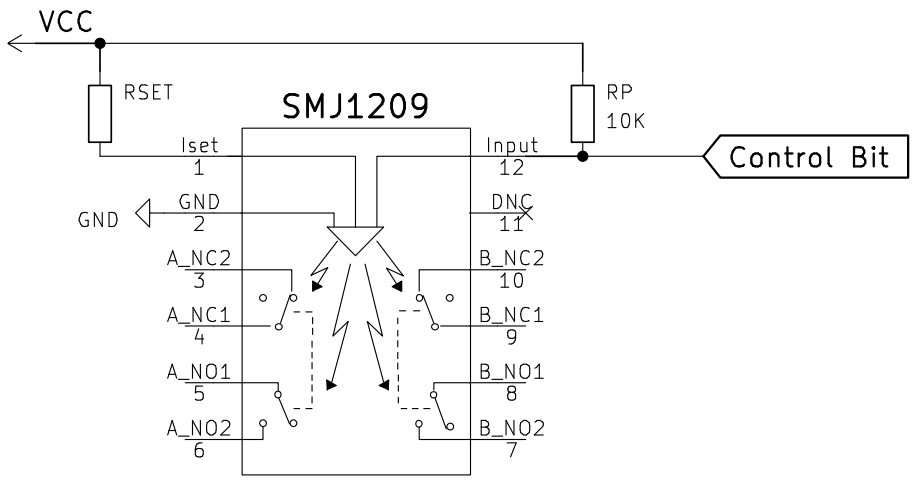


Table 1 below outlines the Operational Truth Table for the SMJ1209 Dual Form C device, per the connections shown in Figure 21 (Basic Functional Circuit). When VCC and ISET are within valid ranges as defined in the Electrical Characteristics Table on page 5, the switch pair closure state is determined by the state of the INPUT pin (pin 12)

A valid INPUT High state occurs when the Control Bit driver is either Open Collector/Open Drain condition and INPUT is pulled up to VCC through RP, or Control Bit drives INPUT to VCC level

A valid INPUT Low state occurs when INPUT is driven below Vin(Low) level as defined in the Electrical Characteristics Table on page 5

All switch pairs will be in an Open state when VCC=0 and ISET=0. This “All Open State” is particularly useful in Multi-Site ATE test circuits for disabling/isolating unused sites

Table 1: SMJ1209 Operational Truth Table

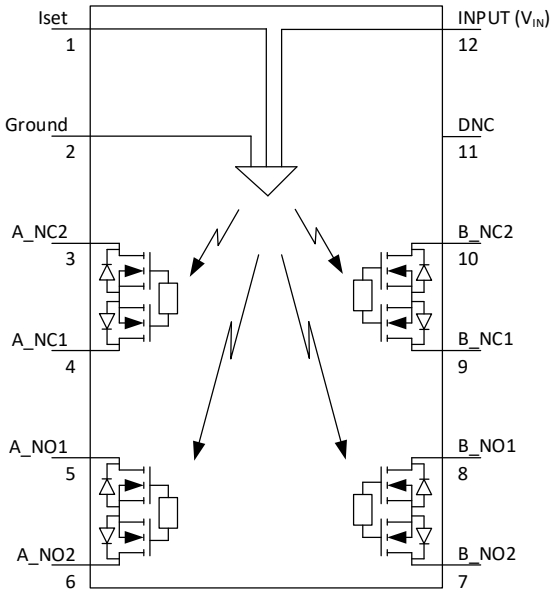
			Switch Pairs			
V_{CC}	I_{SET}	INPUT (V_{IN})	A_NC1 -> A_NC2	A_NO1 -> A_NO2	B_NC1 -> B_NC2	B_NCO1 -> B_NO2
Valid	Valid	OC / V_{CC}	CLOSED	OPEN	CLOSED	OPEN
Valid	Valid	<$V_{IN(Low)}$	OPEN	CLOSED	OPEN	CLOSED
0	0	<$V_{IN(Low)}$ (N/A)[1]	OPEN	OPEN	OPEN	OPEN

Note 1: When VCC / ISET are 0, the INPUT (V_{IN}) does not need to be brought below VINLOW. While the user may opt to do this, it is not required and may be useful in Multi-Site ATE testing where VIN is shared across test sites.

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1 Form C SSR Theory of Operation

Figure 22: SMJ1209 Internal Circuit Detail



The SMJ1209 consists of:

- Two Normally Closed (NC) switch pairs when INPUT = VCC
- Two Normally Open (NO) switch pairs when INPUT = VCC
- ISET Optical LED Control Current setting circuit
- Ground Pin for Control section return currents
- INPUT Logic control for current steering of ISET current to appropriate Optical LED, depending on the threshold state of INPUT pin. The current steering circuit has built-in Break-Before-Make timing to ensure there is no cross-connection of NC-NO switch circuits when changing from one state to another. This Break-Before-Make timing is “Tgap” in the Electrical Characteristics (EC) Table on page 6

The SMJ1209 output MOSFET architecture has a number of advantages over other common industry 2 Form C SSRs which utilize different Form A and Form B technologies. These advantages include and enable:

- Low RON across contact pairs. SMJ1209 typical RON is 500mOhm for all Normally Open and Normally Closed switches. Other solid state relays utilizing Form B switches in a Form C device can have a Form B RON that is 2x that of the Form A companion switch’s RON
- High ROFF for all switch pairs. SMJ1209 open switch ROFF is 80G Ohms @ VB=80V, Ileak=1nA@80V. Traditional Form C SSR relays using a Form A / Form B switch configuration typically have Form B switch Io(leak) much higher than the Form A switch Io(Leak)
- Similar Off State Capacitance (COFF) across open switch contact pairs
- Similar Ton, Toff across switch pairs. This allows the internal current steering circuit to establish Break-Before-Make timing control of switch operation. Establishing tight control of Break-Before-Make timing ensures that signals present on one switch pair do not overlap or cross-connect to other switch pair during state transitions, preventing crosstalk, glitches, and undesired crowbar current spikes in user system resources
- The output architecture of the SMJ1209 device allows a “third state” switch status of “All Open.” Only two functional states are possible with EMR and SSR Form C type devices: The EMR Normally Closed contact and the SSR Form B switch will remain in a closed contact, low resistance state when power is removed from those devices
- The SMJ1209 switches will go to an “All Open” state when power is removed. All NO and NC switches will be in Open state with VCC disconnected. This can be of particular benefit in Semiconductor ATE multi-site testing wherein this state can turn off all other sites with a simple single control. The “All Open” state is discussed in more detail in the Applications section on page 22
- Because a switch pair can be in the “OPEN” state, the SMJ1209 can be utilized as a T-Switch. More details on T-Switch configuration can be found starting on page 24

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Application Information

The SMJ1209 is simple and straightforward to deploy in signal and resource switching applications. The functionality of the SMJ1209 has been designed to closely emulate the operation of legacy electro-mechanical and reed relays, with the intention of replacing these mechanical devices and incorporate the advantages of solid state technology.

Advantages of SMJ1209 SSR over Electro-Mechanical Relays

- Bounce-Free contact switching. Clean transition between Open and Closed states. No chattering of contacts, no downstream circuit disturbance from disruptions in switch path conductivity.
- Predictable and consistent switch Ton, Toff over time. EMR relays tend to increase contact bounce time as they age, necessitating wait times built into system operation to account for EMR Ton, Toff contact settling time from day one.
- Predictable and consistent Ron over time. The SMJ1209 has an Ron Max spec of 750mOhm. EMR relays typically have an Initial Contact Resistance spec of 50mOhm to 150mOhm. EMR Contact Resistance will degrade with use, and eventually reach a point where the system performance will degrade or even fail. In ATE applications, EMR contact resistance creep generally results in ever increasing Device Under Test (DUT) yield loss. This is an insidious source of production line yield loss. As the ATE test circuit EMR contact resistance slowly degrades, production yield losses increase by a few tenths-of-percent over a period of time until yield loss reaches a threshold trip point. Many potentially good DUTs have been discarded by this time. Examining closely EMR datasheets, in some cases, the EMR contact resistance failure point is considered to be 50 Ohms! Few end applications will perform correctly when switch contact resistance increases from 0.05 Ohms to 50 Ohms, thus useful life of EMR can be shorter than expected. The SMJ1209 Ron contact resistance will remain consistent over time and with variable switching loads (loads within device specifications, of course).
- 1 Billion+ switch actuation operating life for SMJ1209. EMR relays typically with have Operating Life Switch Contact specifications of 500K to 5M operations. This is a very short Operating Life for high volume semiconductor manufacturing test, resulting in yield loss and frequent production line down-time. Also with EMR relays, EMR contact resistance degrades faster with higher switching loads. Often EMR datasheets will contain Operating Life vs. Switching Load degradation information, showing that switching at higher loads will significantly reduce Operating Life, with even more frequent down-time than expected.
- No magnetic interference between closely spaced SMJ1209 devices on system PCB. EMR relays typically have a minimum physical keep-away spacing requirement between devices to prevent the magnetic field interference from an activated relay inadvertently activating a relay that is in close proximity, leading to unpredictable system performance. SMJ1209 switch contacts are activated by internal LED light source, not a magnetic field, so SMJ1209 devices can be placed on PCB with minimum keep-out spacing per PCB solderability requirements, saving valuable PCB real estate.
- No Inductive Flyback voltage spike when SMJ1209 control changes state. EMR relay state change is actuated by switching on and off a magnetic field that is generated by current pulled through an inductor coil. When current flow is abruptly cut off in the relay inductor coil, a voltage spike is generated in the coil supply circuit by the collapsing magnetic field. This spike can reach 100's of volts and will cause cross-talk in cabled systems if the excursion is not clamped by a suppression diode placed across the relay coil.
- No Dissimilar Metal Thermal EMF Generators Across Contacts. Electro-Mechanical Relay contacts are plated with varying metal types. When dissimilar metals are in physical contact, a parasitic Thermal EMF is generated in series with the electrical connection. The Thermal EMF generated by the metallic contacts will manifest as a time and temperature varying DC offset in the circuit. Depending on contact metal plating types, Thermal EMF can range from <10uV to greater than 100uV. EMR Relay Contact Thermal EMF can be a significant source of DUT measurement correlation error and poor R&R when testing devices such as OpAmps, DACs, ADCs when the inherent DUT DC Offset can be of similar value as the relay generated Thermal EMF. The SMJ1209 avoids this source of test measurement error, and has no metallic switch contacts to form Thermal EMF generators.

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Application Information (continued)

Advantages of SMJ1209 SSR over Analog Switches

The SMJ1209 presents a number of advantages in test circuit and signal switching over Analog Switches:

- Galvanic isolation between the control side and signal side of the relay. SMJ1209 SSR uses LED light transmission to control the operation of switch pairs. Power domains between control side and signal side can be completely independent.
  - Analog Switches share a common power and ground connection between Control and Signal side
  - The common power and ground can result in parasitic leakage paths between the Control circuit and Signal circuits
  - Common power and ground can result in Control power supply ripple feeding through to the Signal path by modulation of Ron vs supply voltage
- Galvanic isolation helps prevent ground loop creation between Control and Signal circuits in the system by allowing independent power domains and ground returns
- High Common Mode Voltage Isolation between Signal side and Control side of relay. The common mode withstanding voltage of the SMJ1209 is 300VRMS between Signal to Control side of the relay. The SMJ1209 can switch signals that are riding on up to 300V common mode voltage separation from Control side power domain.
  - Analog Switch common mode voltage isolation is typically limited to the operating power supply span present on the VDD and VSS pins of the Analog Switch. VDD-VSS span of Analog switches is typically +/- 5V to +/- 15V
- Switch On Resistance (Ron) value independent of Signal common mode voltage. Since the bias source for “On” switches is photons of light, the SMJ1209 switches have no way of “knowing” what common mode voltage level the desired signal is riding on.
  - Analog Switches typically have an “Ron Flatness” specification that describes how Ron changes with Signal common mode voltage levels
- Higher current carrying capacity than Analog Switches. The SMJ1209 can carry 750mA steady state and pulsed currents up to 2A at 25°C
- Low Signal-to-Ground capacitive coupling. The SMJ1209 Signal-to-Ground capacitance is driven by the physical size and spacing of the package contact pads, typically <1pf.
  - Analog Switch Signal-to-Ground capacitance is much higher. CD(On), CD(Off), CS(On), CS(Off) are typically range from 20pf to >>100pF for similar Ron devices

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Application Information (continued)

Replacing or Retro-Fitting EMR Relays with SMJ1209 SSR in Applications

Given the important use-case advantages noted above that SMJ1209 Solid State Relay provides over Electro-Mechanical or Reed relays with similar functionality, the user system operating circuit conditions need to be considered when retro-fitting into existing legacy system boards.

For the end user to realize all of the advantages of replacing EMRs with SSRs, engineering judgement and analysis must be applied. Below is a list of many, but not all, engineering considerations to evaluate when retro-fitting or replacing EMRs with SSRs in a circuit. There are general, overall SSR retro-fit considerations, and additional considerations specific to ATE/Semiconductor Test applications.

General SSR Application Considerations:

- Breakdown/Blocking Voltage (VB) between Open switch contacts: EMR relays used in ATE test applications typically have Open switch breakdown voltage ratings of 200-500V, so open contact breakdown voltage rating is rarely considered when designing an ATE test schematic with EMRs. The switch dielectric for EMR Open switch is essentially an air gap. Solid State Relay switch elements are generally made up from MOSFET semiconductor devices, so the Blocking Voltage (VB) specification takes into account the geometry of the MOSFET device. Depending on the MOSFET size vs. Ron vs. VB tradeoffs in the SSR design, the SSR Blocking Voltage (VB) can typically range from 20V to 300V. When retro-fitting or replacing EMRs with SSRs, a very detailed understanding of circuit voltage levels that will be presented across the SSR contacts must be worked up, so the correct SSR device can be selected. The SMJ1209 has a VB specification of 100V. (SSO offers a selection of Form C SSRs for ATE Testing with VB ranging from 60V to 250V - see page 29)
- Open Contact Leakage Current (ILeak): Since the Open contact of an EMR is an air gap, Roff of an Open contact is very high, typically >> 100G Ohm, and only limited by the insulation resistance of the relay package. SSR MOSFET devices have an Open switch contact profile of a depleted N-channel MOSFET device. That is, leakage current across the Off (Open contact) MOSFET will follow an IDSS curve: I(Leak) gradually increases as VB increases, until MOSFET breakdown voltage is exceeded, and Ichannel exponentially increases. The SMJ1209 I(Leak)@100V is specified at 100nA, which corresponds to Roff of 1G Ohm @100V; I(Leak)@80V is specified at 1nA, which corresponds to Roff of 80G Ohm @80V. When the SMJ1209 is operated with VB less than 10V, the I(Leak) will be typically be less than 100pA. Some test circuit designers will select 100V VB specified SSR's for use in 10V circuits to achieve this lower I(Leak) performance. As 100pA current levels are not practical to measure in high speed automated semiconductor test manufacturing, I(Leak)@10V is noted here as typical only information.
- Open Switch Capacitance Across Contacts (Coff): EMR Open switch contacts are physically separated across an air gap, resulting in low Coff, typically <1pF. The Coff of SSR MOSFET is driven by the device geometry, which in turn is driven physical size, Ron, VB considerations. Coff for SSR MOSFET will be highest when 0V is across the Open contacts, Coff lowest when VB voltage is across the Open contacts. The Electrical Characteristics Table lists typical Coff vs VB values for SMJ1209.
- Switch Contact Resistance (Ron): EMR relays are typically specified with Initial Contact Resistance specification in the range of 0.05 – 0.15 Ohms. This EMR Initial Contact Resistance typically degrades over time and number of switch actuations, with contact resistance degradation occurring at a faster rate as the switching load increases. EMR contact resistance degradation drives the Operating Life specification for these devices. Close examination of footnotes in some EMR datasheets notes that criteria for failing contact resistance value to set end of Operating Life number can be as high as 50 Ohms. In addition, some EMR datasheets will list Dynamic Contact Resistance, which is the peak-to-peak modulation in contact resistance that is caused by switch contact vibration and mechanical flexing that occurs for some time after the switch mechanism stops bouncing. In highly sensitive circuits, this could manifest as bursts of noise in the signal through the contact Ron value modulation during this time period.

ATE and Semiconductor Test Application Specific Considerations:

- A determination must be made if SMJ1209 SSR Ron of 750milliOhms is of significant magnitude or can be ignored for specific test circuit performance criteria. SMJ1209 SSR RON impact on test measurement results can be mitigated, either through calibration, computation, or Kelvin sensing. It is important to note that SSR RON remains low and stable over time.
- ISET Return Current management: For an EMR, the control coil return current from the Relay Power source is routed back through the relay driver's low impedance output stage pull-down to system ground. Therefore, no Ground pin required for EMR relay functionality. The SMJ1209 SSR ISET current does require a Ground pin for SSR power source return currents, as the NC - Form B switch LED is powered up while the device is in the idle state (INPUT=VCC). The system relay driver output stage is in high impedance state when pulling-up to VCC, so the ISET Optical Control Current requires an alternate return path to system Ground . This is provided by the Ground pin on the SMJ1209 package. The SMJ1209 Ground pin requirement is a notable difference that must be managed when replacing or retro-fitting EMRs with SMJ1209 in existing legacy application circuits. An ability to connect Ground pin of the SMJ1209 to system ground must be worked into retro-fit applications. For new PCB designs or re-spinning legacy PCB designs, the inclusion of SMJ1209 Ground pin connection can be designed in from the start.

Application Information (continued)

- Ground Return Current Management in cabled (soft-dock) systems: If a test board fixture is a cabled or "soft-dock" design, where the DUT test fixture is a separate PCB and then is connected with cables or wires back to the ATE system, care must be taken with managing the ISET ground return currents of the SMJ1209's mounted on the remote test fixture. The ATE system resources and the SMJ1209 devices should have either robust (low resistance) ground return path, or independent ground return wires/connections for the system resources and the SMJ1209 devices in cabled systems. The reason being:

  The sum of the ISET currents can cause IR voltage drops in the ground return line due to the series resistance of connectors and cables. For example, if an ATE system DVM low side is grounded at the ATE test head, then shares the ground return line from the remote PCB with these ISET return currents, the resulting IR voltage drop can manifest as a DC offset in the DVM readings and become a source of correlation error. Say the soft-dock remote test fixture PCB has 10 SMJ1209's installed @5mA ISET each (ISET of 5mA is sufficient to drive each SMJ device with TON of ~800us). Then up to 50mA of total return current can be present on the ground return path, depending on relay activation state. In this example, if the low side return path wiring and connectors has 100mOhms of series resistance, then a 5mV IR drop will develop end to end. It is best practice to Kelvin sense the low side of the DVM up to the remote PCB test fixture in any case, but legacy designs need to be checked for this potential source of measurement error. In Kelvin sensed PCB designs with well managed ground pours and planes, this is not an issue.

Setting Component Values for Operational Supply Voltage Range

The SMJ1209 has an Operational Supply Voltage Range of 4.5 – 16.0V. This enables the device to retrofit into a wide spectrum on Electro-Mechanical Relay (EMR) legacy replacement use cases. The SMJ1209 is compatible with Open Drain, Open Collector, and Darlington legacy relay drivers, provided the output stage of the driver pulls below SMJ1209 VIN(Low) level of 1.1V when relay driver is activated.

An RSET resistor must be selected to result in the desired ISET for the switching application. ISET operational range is 3mA – 12mA with guaranteed Break-Before-Make switch open-close timing. The optimal ISET value is 8mA.

Typical Operating Curves for TON and TGAP are shown in Figures 10 - 13 (page 8) to help user select optimal ISET value per application.

The ISET value selection trade-offs include: switch operational timing Ton, Toff, TGap , device power consumption as the SMJ1209 ISET current is constant while device is powered up. EMR devices generally only consume power when the relay driver is in active Low state, no power consumption in the idle (pulled High) state.

The user must decide on ISET values that are optimal for a particular application. Lower ISET values save input current while increasing the TGAP and TON times. Higher ISET values result in faster TON and lower TGAP times and can be used where the user requires faster speeds. Reference "Coupled Specifications" section of the Electrical Characteristics table on page 6. The nominal ISET value of 8mA is suitable for most applications.

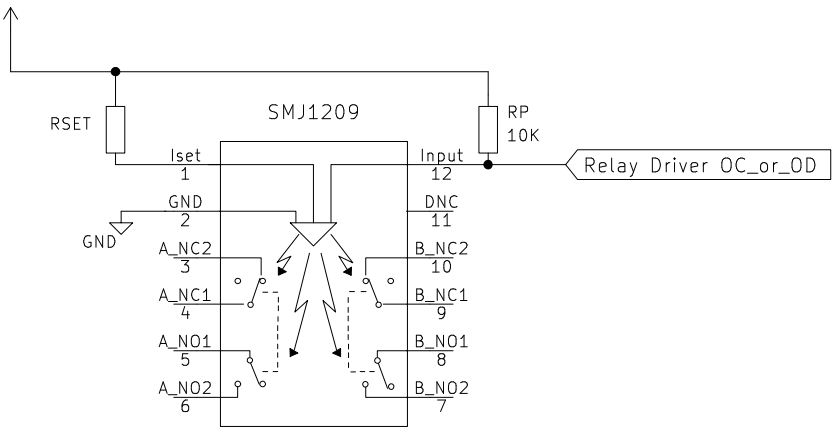
The equation to compute RSET to yield a target ISET value is: RSET= (Vcc-2.15) / (ISET(target)). See note 5 on page 11 for sample RSET Calculations for ISET = 8mA.

RSET can be selected to nearest 5% standard resistor value if RSET computed does not align with a standard value.

Figure 23: RSET Values / SMJ1209 Input Circuitry

RSET vs VCC for ISET = 8mA

VCC	RSET (5%)
5.0V	360 Ohm
8.0V	750 Ohm
12.0V	1.2K Ohm
15.0V	1.6k Ohm



Application Information (continued)

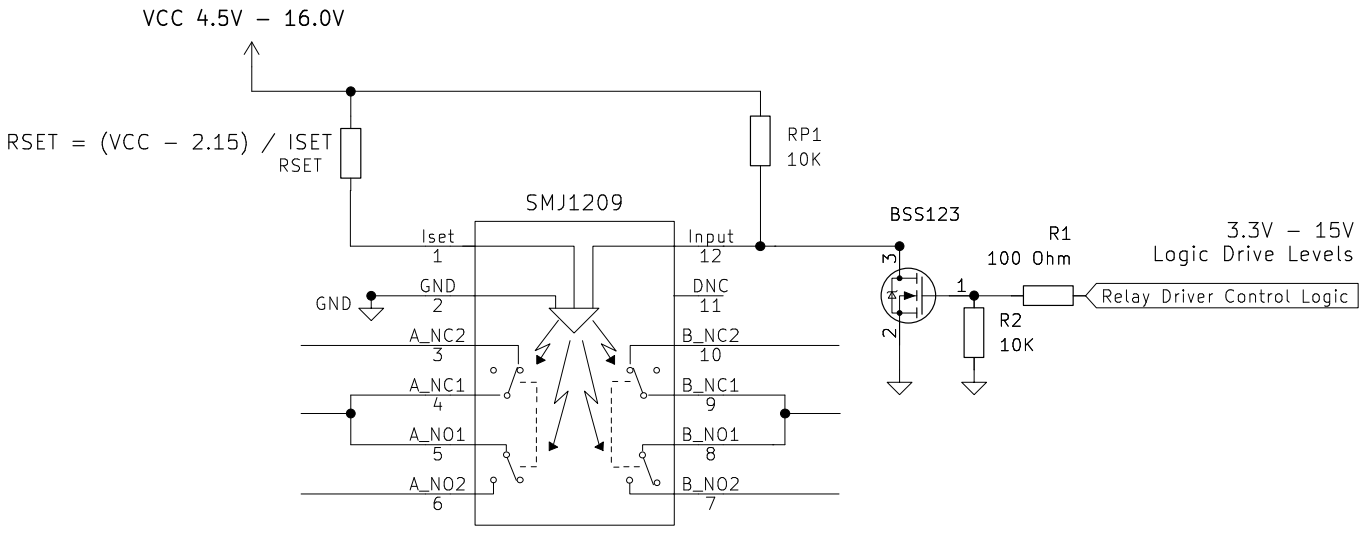
Controlling SMJ1209 with Open Collector / Open Drain Drivers

Automatic Test Equipment (ATE) systems used in semiconductor manufacturing test, generally have Open Collector or Open Drain Relay Control Bits (CBit) banks used for driving legacy Electro-Mechanical Relays (EMRs). These legacy OC or OD CBit drivers can be used to drive the SMJ1209 Solid State Relay (SSR). The user should place a 10K pull-up resistor to VCC on the PCB close to the SMJ1209 so that the device will have a definite pull-up resistor on the INPUT pin to VCC in the event that connection to the ATE system CBit driver becomes open. This will prevent the INPUT pin from floating and having an indeterminate threshold condition.

The ATE system Cbit driver VCESat Open Collector saturation voltage or the Open Drain driver output stage ((RON)* (total load ISink)) must result in a voltage at the SMJ1209 input pin of less than specified VIN(Low) of 1.1V for the device to function correctly when the CBit driver pulls down. Legacy ATE CBit drivers generally meet this requirement easily, as EMR relays operate at higher currents than SSR devices. Users should review the specific ATE platform specifications for CBit driver VCESat or Open Drain RON to ensure correct functional operation of SMJ1209 devices when CBit output is low.

Legacy EMR relays generally require a fly-back diode across the control coil, due to the inductive kick-back voltage when the EMR is deactivated. The SMJ1209 SSR does not require a fly-back diode in the control circuit, as no inductors/coils are involved with the control circuit. If the legacy circuit has the flyback diode installed, it can be left in place.

Figure 24*: SMJ1209 Controlled by Open Drain Driver*



Application Information (continued)

Controlling SMJ1209 with other Logic Families

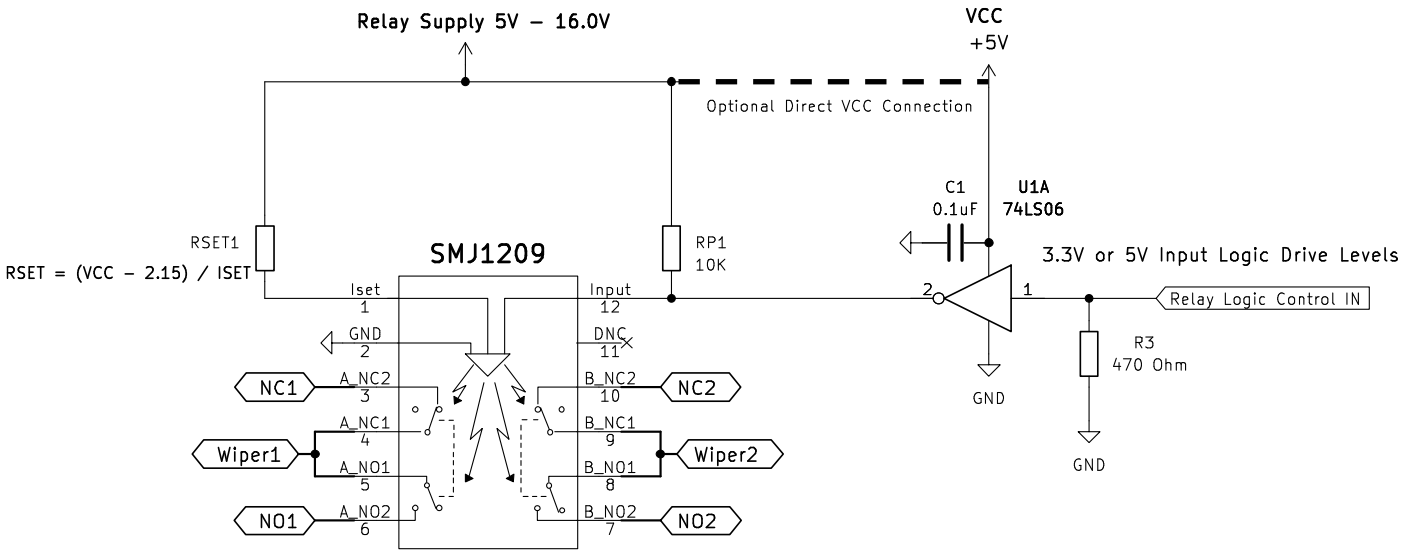
The SMJ1209 can be controlled by logic families other than Open Collector or Open Drain Relay Drivers found in Automatic Test Equipment (ATE)

Low Power Schottky -- 74LS Logic with Open Collector:

3.3V logic is very common in microcontrollers and single board computers such as Arduino and Raspberry Pi. The SMJ1209 can be interfaced with 3.3V logic devices using a level translator such as the 74LS06 Hex Open Collector Inverter. The 74LS06 is a Low Power Schottky TTL device with 3.3V logic and 5V logic tolerant inputs. The 74LS06 Open Collector output is rated up to 30V tolerant, allowing the 74LS06 to work with the SMJ1209 over its 4.5V to 16.0 VCC Operating Range, giving maximum flexibility for user system relay power supply levels. A 470 Ohm pull-down resistor is placed on the input to the 74LS06 to ensure that the output returns to a high (idle) state if the input logic drive is disconnected.

The 74LS06 has sufficient output sink current that each LS06 channel can control multiple SMJ1209 Input lines in parallel, number depending on ISET value used for each device (each SMJ1209 has its own 10K Input Pull-Up per device).

Figure 25: SMJ1209 Controlled by 3.3V or 5V Logic Input with 74LS06 Hex Open Collector Driver Compatible with System Relay Power Supplies >5.5V



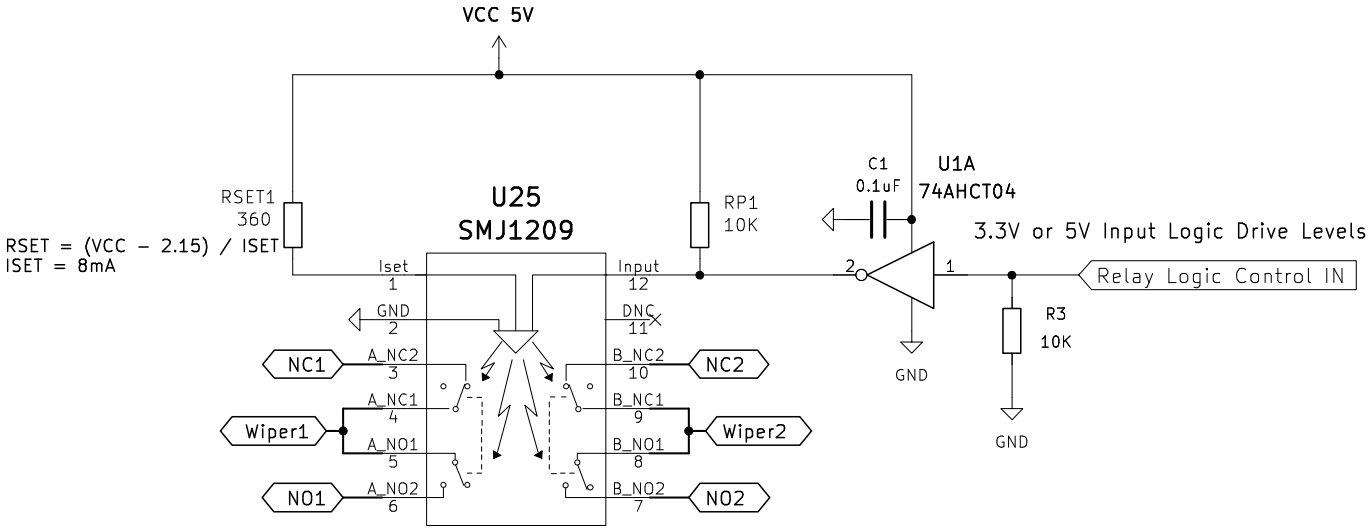
Application Information (continued)

74AHCT—Advanced High Speed CMOS TTL Compatible Logic Drivers:

The SMJ1209 can be directly driven by 74AHCT Logic devices. The 74AHCT device must be powered from the same 5V supply rail as the SMJ1209, and the Pull-Up resistor RP on the output of the 74AHCT device reduced to 5K Ohms.

- User should note that if 3.3V logic is driving the input to the 74AHCT device, the 74AHCT device will draw elevated Icc currents of ~1.5mA per channel when inputs are driven to 3.3V levels. The user needs to ensure that 5V system supply can provide the increased current demand when interfacing 3.3V logic with 74AHCT devices
- If 5V logic is driving the input to the 74HCT device, the 74HCT device supply current will be at nominal value

Figure 26: SMJ1209 Direct Drive Control with 74AHCT04 Hex Inverter Compatible with 3.3V or 5V Logic Levels



Application Information (continued)

1.8V Microcontroller Interfaces:

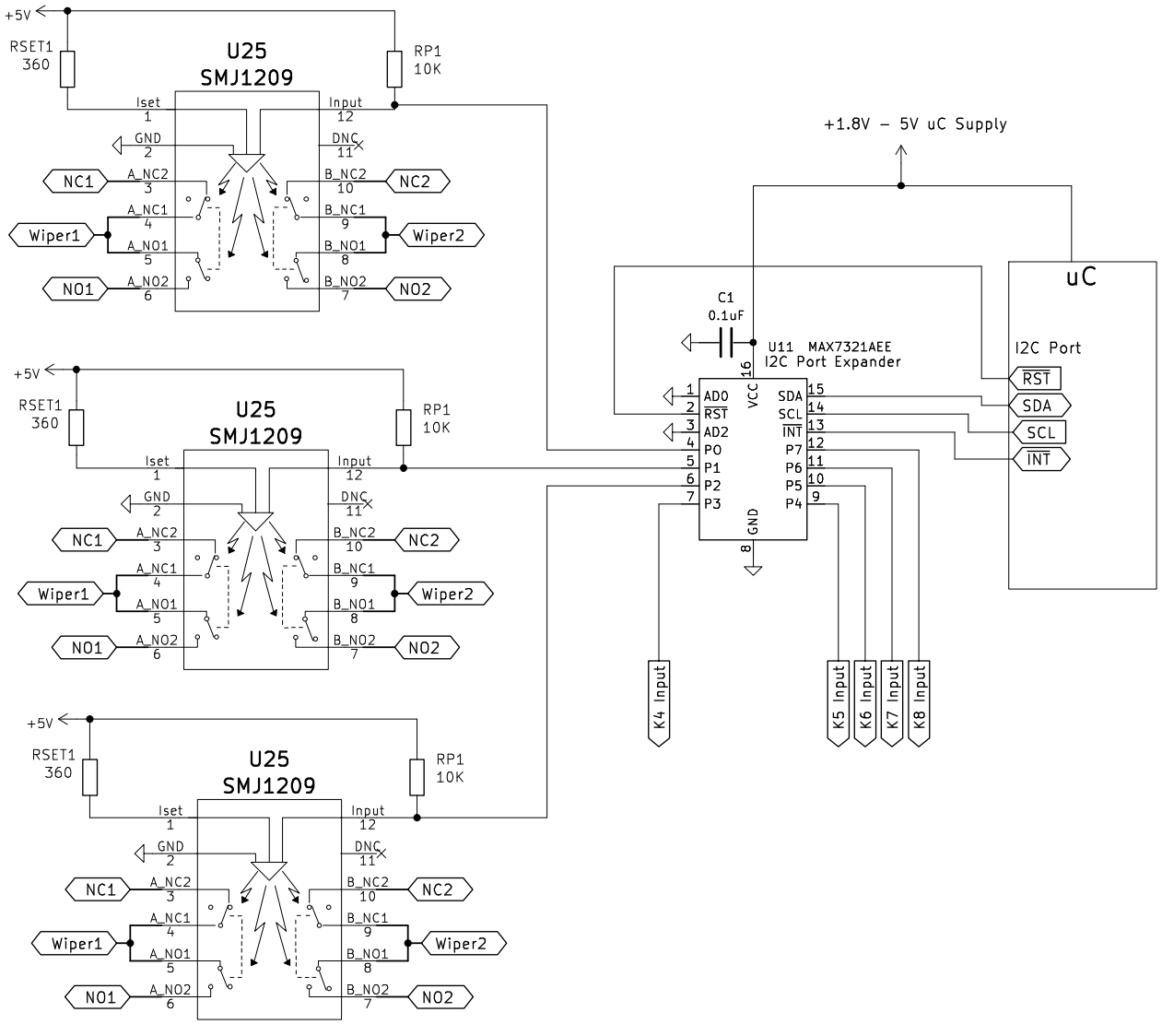
Many Single Board computers use low voltage (1.8V) microcontrollers for the engine. The 1.8V logic levels from these microcontrollers' interfaces are too low to set valid logic levels for 74xxx series drivers and other buffer types. The 1.8V logic levels can also be marginal for directly driving the gates of discrete MOSFETs that would serve as Open Drain drivers for the SMJ1209.

One option is to use a 1.8V compatible I2C I/O Expander with Open Drain outputs controlled by communications ports on the microcontroller. Figure 27 below shows one such example with a MAX7321 8x Open Drain I/O Expander driven by the microcontroller I2C bus interface.

The I/O Expander is powered from the same VCC supply as the microcontroller to ensure logic level compatibility on the communication port. The Open Drain outputs are pulled up by the 5V supply for the SMJ1209 SSRs.

The example shown is with an I2C interface port. Similar I/O Port Expanders exist for SPI and other interfaces. Select an Expander that has sufficient IOL sink capability for SMJ1209 ISET current.

Figure 27: *SMJ1209 Driving Multiple SMJ1209 SSRs with 1.8V MicroController I2C Interface*



Application Information (continued)

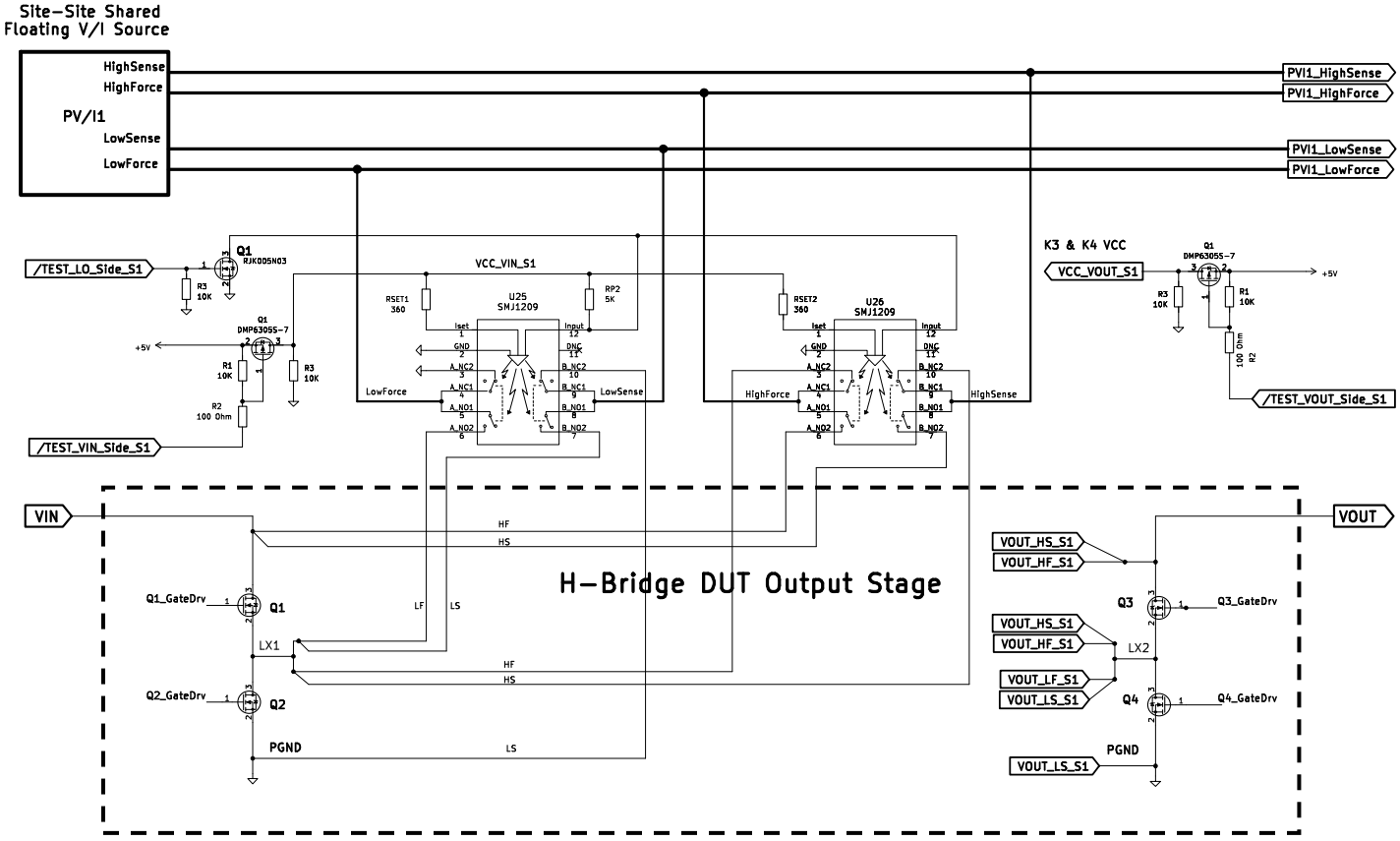
Third Operating State - Using "All Switches Open" Mode to Reduce Relay Count in Multi-Site Loadboards

Another advantage of the SMJ Dual Form C relays is the third functional state of "All Switches Open." Standard EMR and Reed Form C relays have just two stable states: Normally Closed and Normally Open switch contacts. In an EMR or Reed relay, one switch pair is always closed. With the SMJ1209 device, when the ISET and Input control circuits are de-powered, all switch pairs in the device will go to an Open state, thus the third functional state "All Switches Open" is available.

The "All Switches Open" state is particularly useful in multi-site ATE test applications where an ATE resource, such as a Power V/I channel, must be shared across multiple sites. The test circuit using EMR or Reed relays will need Dual Form C Kelvin Force - Sense relays, plus Site Isolation Dual Form C relays that enable site-site resource sharing. In the case of the H-Bridge Output RON test shown below, using the SMJ device "All Switches Open" feature allows the Kelvin Force-Sense and Site Isolation functions to be combined into a single device, thus saving four Dual Form C devices per site. In an Octal site ATE board, this results in a reduction of 32 Dual Form C relays from the BOM count, reducing cost and complexity from the ATE loadboard.

For the sake of clarity, only the VIN side of H-Bridge test circuit is shown below. VOUT side and additional DUT sites are repeats of this circuit configuration.

Figure 28: Octal Site ATE Loadboard Utilizing "All Switches Open" State



Application Information (continued)

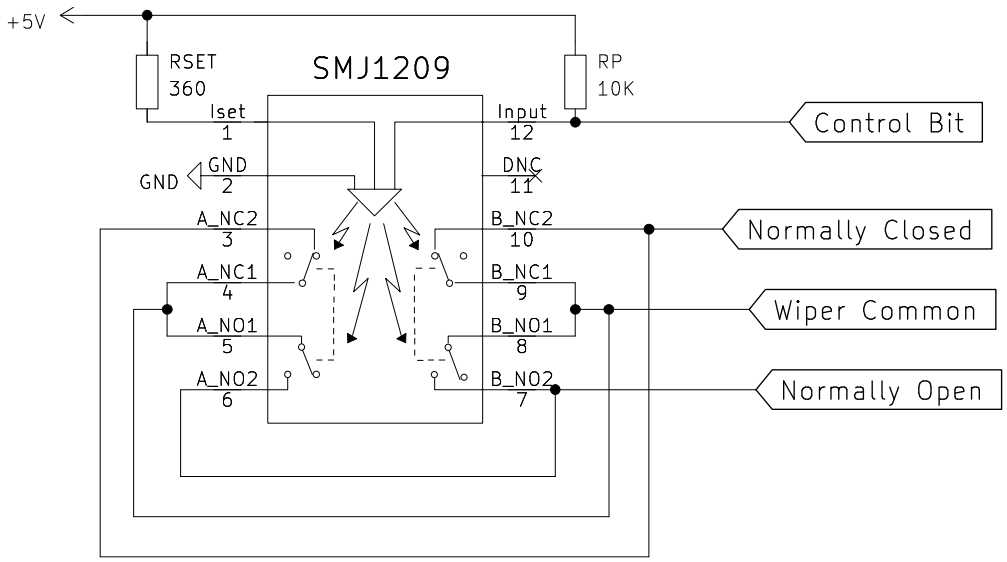
Paralleling Dual Form C Switch Pairs for Higher Current Carry Capacity

The switch pairs in the Dual Form C devices can be externally connected in parallel as shown below in Figure 29. This will form a Single Form C relay that achieves 2x higher current carry capacity should the end application require higher current load capability.

For example: The SMJ1209 Dual Form C load current rating per switch is 750mA continuous and 2A pulsed @ 10% duty cycle. If the switch pairs are connected in parallel, the current carry capacity of the resultant Single Form C relay contacts are 1.5A continuous, 4A pulsed @ 10% duty cycle, 100ms period.

Current hogging in the parallel switches is not a concern. The paralleled switches of the SMJ1209 are inherently current balancing. The RON of the SMJ1209 switches have a positive temperature coefficient. The paralleled switch with the lower initial RON will carry more current initially, will dissipate more power until its RON elevates and comes into balance with its paired switch's RON.

Figure 29: Paralleling Dual Form C Switch Pairs Increases Current Capacity



Application Information (continued)

T-Switch Configuration Reduces SSR DC Leakage and AC Signal Feedthrough

An additional function that can be realized with the SMJ Dual Form C devices is that of a T-Switch.

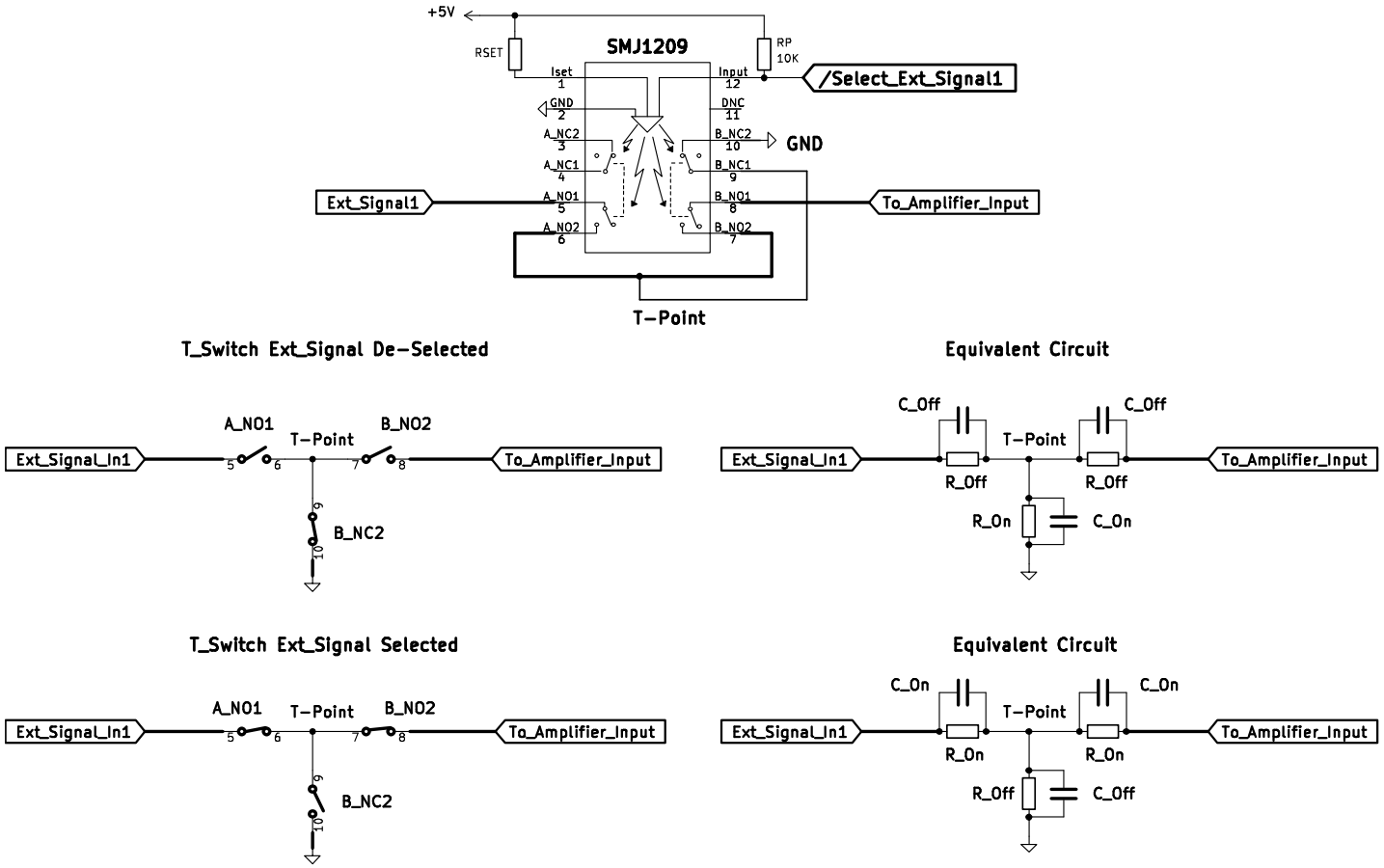
A T-switch implementation can overcome a number of limitations of Form A Solid State Relays:

- Greater than 3x orders of magnitude reduction in open switch leakage current.
- 100dB + reduction in AC signal feedthrough vs. Form A is achievable.

The T-Switch configuration DC leakage and AC signal feedthrough prevention in signal switching rivals the best of Reed relays performance.

Figure 30, shown below, depicts how to externally connect the pins of an SMJ device for T-Switch functionality. The T-Switch function makes use of three of the four internal switches. The switch operation function is ganged internally to achieve the proper Break-Before-Make timing of switch open and closures. This prevents any closed switch overlap. The mid-switch connection to ground at the T-Point intercepts DC leakage and AC feedthrough coming in from the input signal side and prevents passing through to the output side of T-Switch.

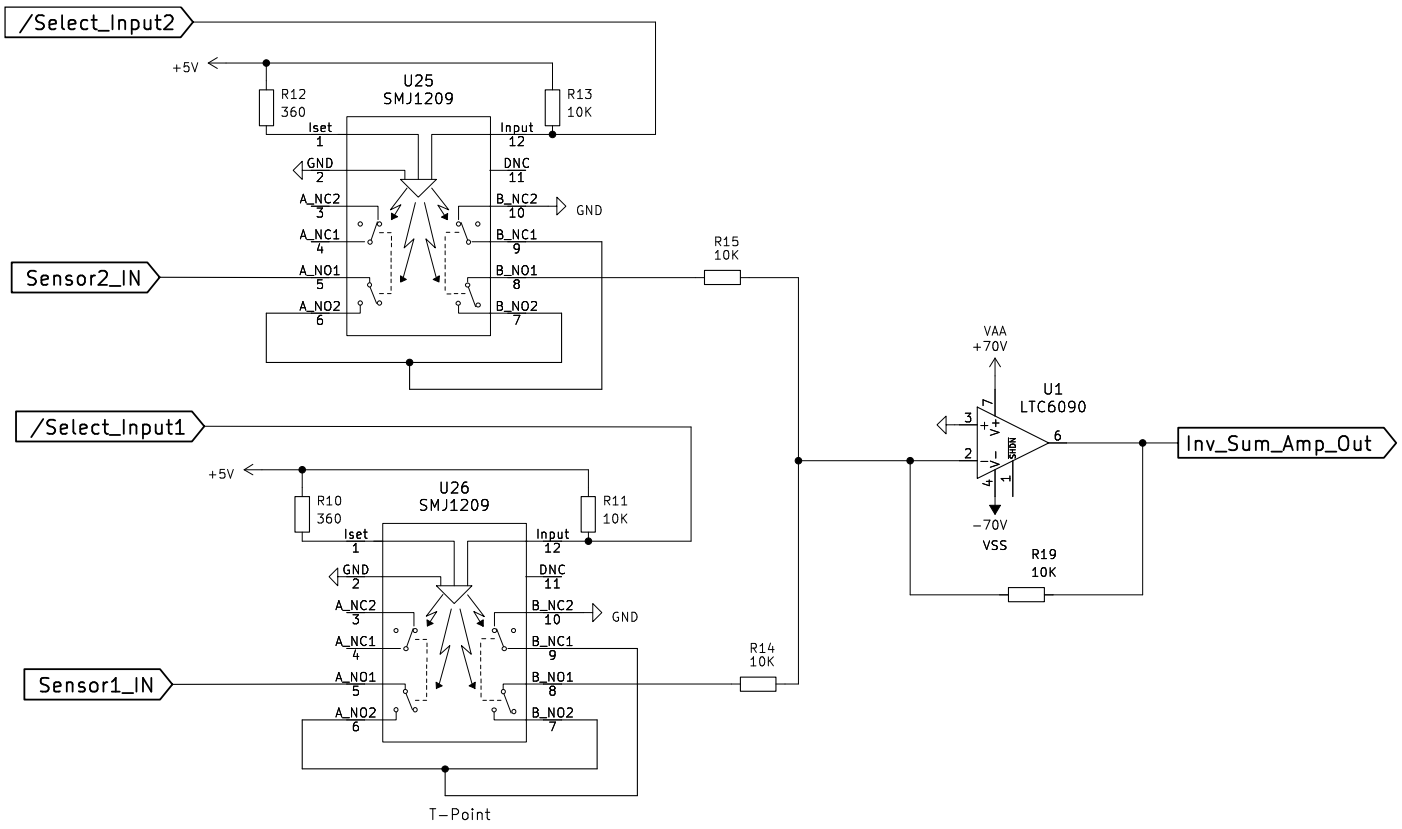
Figure 30: T-Switch Configuration



Application Information (continued)

A T-Switch implementation of a 2 input High Voltage Summing Amp is shown below in Figure 31. The SMJ1209 in a T-Switch configuration enables high DC and AC isolation from de-selected signal inputs to OpAmp and minimizes crosstalk between multiple input stimulus sources.

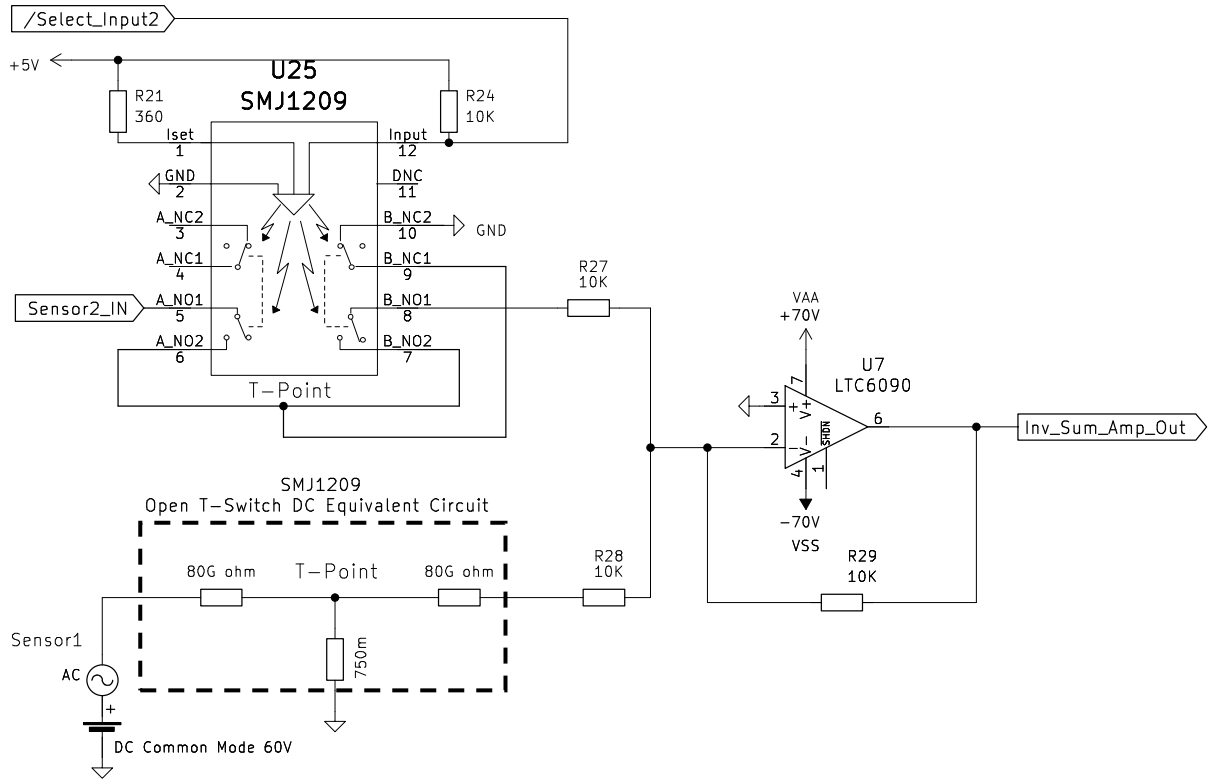
Figure 31: 2 Input HV Inverting/Summing Amplifier with T-Switch Isolated Inputs



Application Information (continued)

The DC Equivalent circuit shown below in Figure 32 demonstrates how the DC leakage currents from input signal source to the inverting input of the amplifier are reduced in a T-Switch over single Form A SSR. The open switch of the SMJ1209 SSR can be modeled by an 80G ohm resistance when open switch Blocking Voltage (VB) is less than 80V. In the example below, if a single Form A SSR switch is used for Mux switch, then Ileak into the amplifier would be 60v/80G Ohm = 750pA. Using a T-Switch connected input switch, the 80G ohm of the A_NO open switch forms a voltage divider with the 750mili Ohm Ron of the B_NC grounded switch to yield near zero volts at the T-Point. Therefore, the total voltage across the open B_NO switch resistance of 80G ohm is essentially the input offset voltage of the U3 amplifier. The LTC6090 Vos is typically 1mV, so resulting DC leakage into the amplifier feedback network from the de-selected input path blocking a 60V signal calculates to less than 1pA. Actual DC leakage observed with this circuit will be dominated by PCB surface resistivity and layout techniques.

Figure 32: 2 Input HV Inverting/Summing Amplifier with T-Switch Isolated Inputs

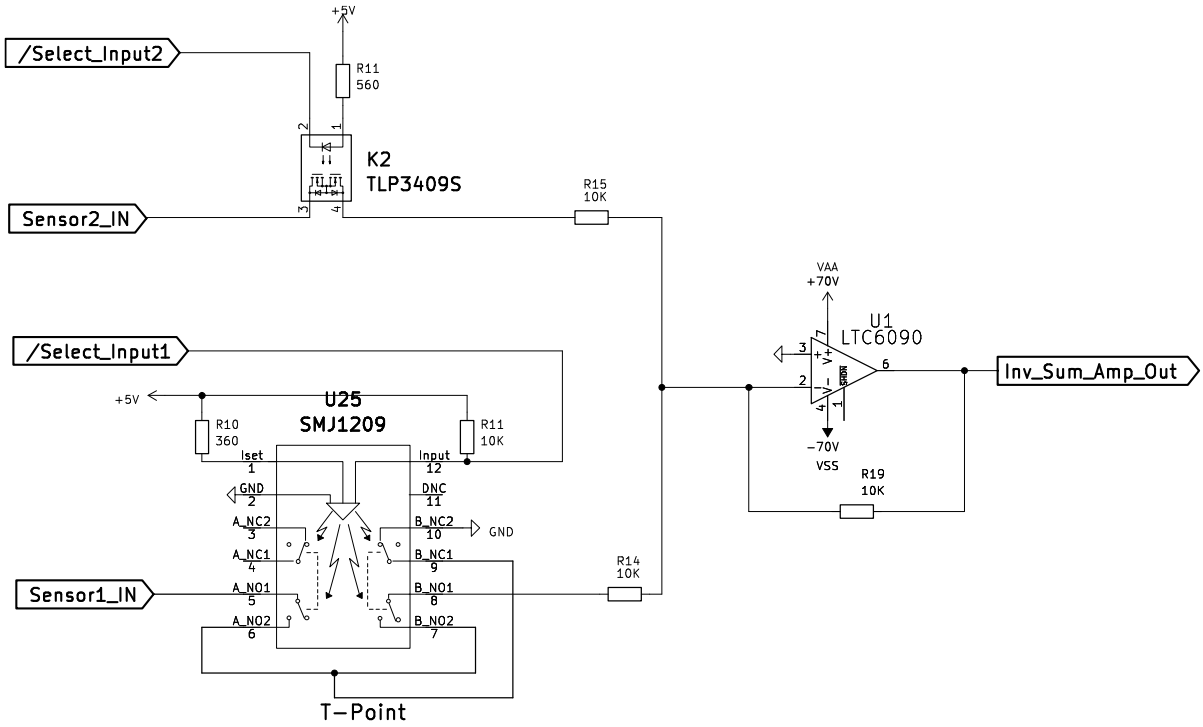


The best circuit design practice is to place the T-Switch on the sensor input side of the input summing resistors (R27 and R28 in Figure 31, previous page), and not on the summing junction side. In this way, the input summing resistors will isolate the SSR switch capacitance from the OpAmp input circuit. Many OpAmps are sensitive to input capacitance on summing junction node. Series ordering the SSR and input resistors in fashion shown above avoids capacitive loading on the OpAmp input node.

Application Information (continued)

The T-Switch configuration input mux offers significant crosstalk reduction over Form A SSR mux configuration. Figure 34 below compares the unwanted signal feedthrough with a standard Form A SSR Mux switch vs T-Switch configured SMJ1209. The signal feedthrough with the Form A input Mux switch becomes excessive at relatively low frequencies while T-Switch mux maintains high isolation characteristics vs input signal frequency.

Figure 33: 2 Input HV Inverting/Summing Amplifier Form A vs. T-Switch Isolated Input



If we assume a system 16 bit ADC with 96dB of dynamic range is connected to summing amp output with 0V Common Mode voltage, then the DC leakage and upper useable frequency limits for an input mux using Form A SSR with specifications of : DC leakage =1nA @80V, Coff = 75pF @0VCM vs SMJ1209 T-Switch are listed in the Table below.

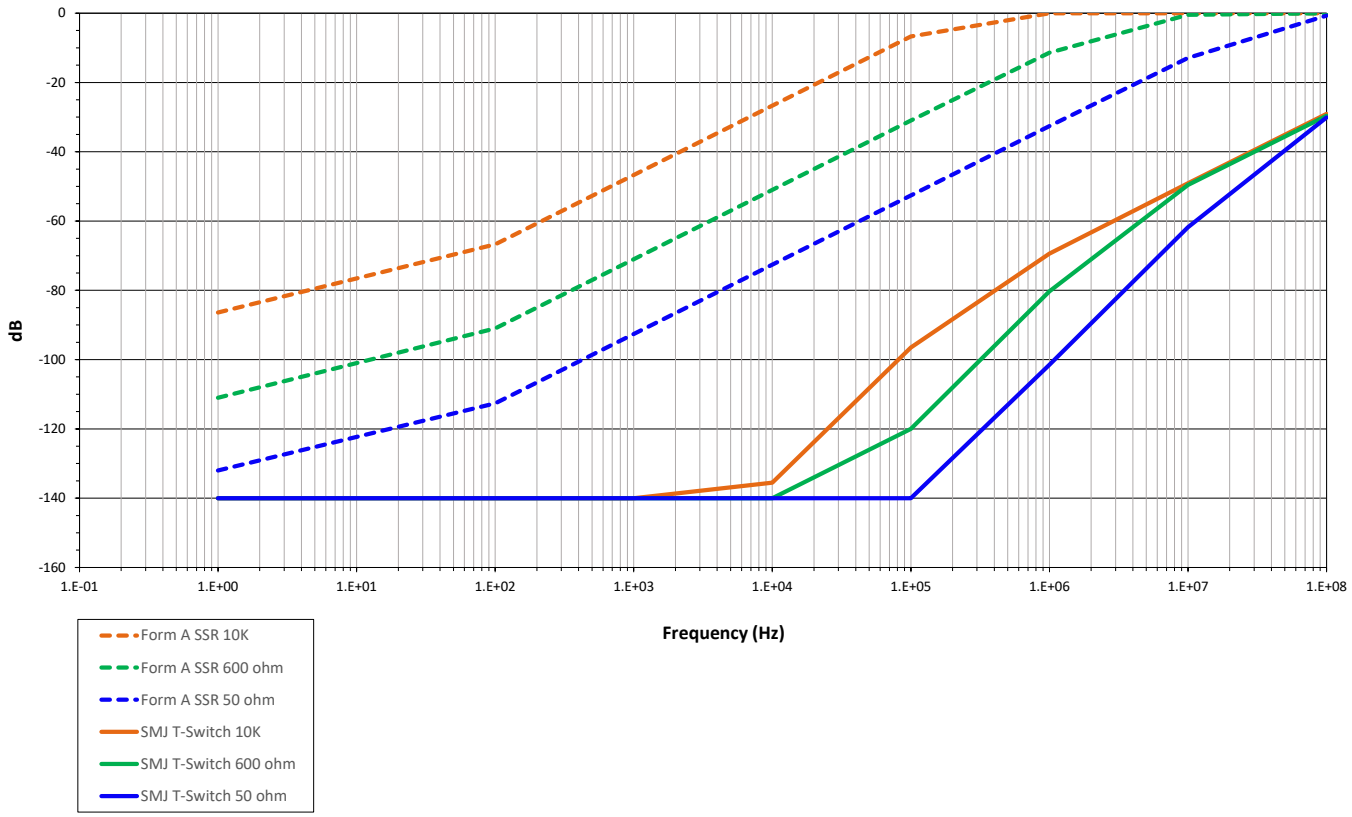
Table 2: SMJ1209 T-Switch DC Leakage & Usable Frequency

MUX Type	**DC Leakage** VB = 60V	**Input Impedance** 10k Feedthrough < 96dB	**Input Impedance** 600Ω Feedthrough < 96dB	**Input Impedance** 50Ω Feedthrough < 96dB
Form A SSR SPST	750 pA	1 Hz	50 Hz	700 Hz
SMJ1209 T-Switch	<1 pA	100 KHz	400 KHz	1.4 MHz

Application Information (continued)

The T-Switch mux configuration offers 3-4 orders of magnitude reduction in DC leakage and AC feedthrough as compared to a comparable Form A SSR switch. A comparison between AC feedthrough with Form A SSR vs SMJ1209 T-Switch into various amplifier impedance terminations is shown in the graph below (Figure 34).

Figure 34: Off Channel Feedthrough vs. Frequency—Form A SSR vs. SMJ1209 T-Switch into 10K, 600Ω, 50Ω Impedance



Using the SMJ1209 in a T-Switch configuration for signal switching applications can overcome many limitations of Form A SSR signal switches and enhance overall circuit performance. T-Switch configuration achieves orders of magnitude reduction in DC Leakage and AC signal feedthrough, rivaling the best signal switching performance of reed relays while offering the advantage of enhanced reliability, durability and extended operating life.

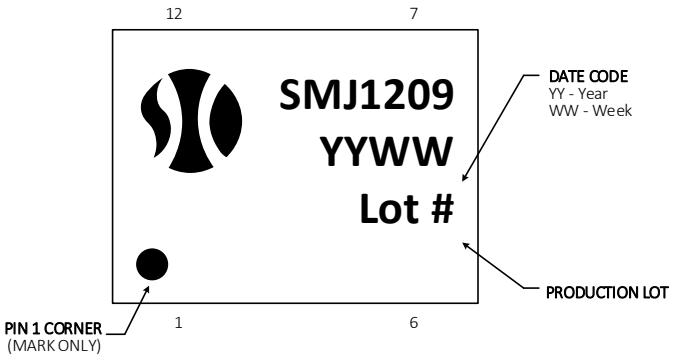
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Table 3: Product Family Offering

Product	Electrical Specifications									Package Specifications				
	V_B	I_{LOAD}	I_{LOAD}	R_{dsON}	I_{LEAK}	V_{ISO}	C_{OUT}			Type	L	W	Area	H
	MAX (V)	MAX (mA)	Pulsed (mA)	TYP (Ohms)	@V_B-20V (nA)	MIN (V_{RMS})	V_O = 0 (pF)	V_O = 25 (pF)	V_O = 60 (pF)		(mm)	(mm)	(mm^2)	(mm)
1 FORM C (Single Channel)														
SMC1309	100	750	2000	0.500	1	1500	75	18	12	SOP8	9.4	4.4	42	2
SMC8609	100	750	1500	0.500	1	300	75	18	12	DFN8	6	5	30	3
SMC8619	200	550	1100	1.300	1	300	85	20	12	DFN8	6	5.5	33	3
SMC8629	250	450	900	3.500	1	300	70	18	10	DFN8	6	5.5	33	3
SMC8659	60	1000	2000	0.175	1	300	90	20	-	DFN8	6	5	30	3
SMC8660	60	250	500	7.000	1	300	26	8	-	DFN8	6	5	30	3
2 FORM C (Dual Channel)														
SMJ1309	100	750	2000	0.500	1	500	75	18	12	SOIC16	10.4	9.2	96	2.1
SMJ1359	60	1000	2000	0.175	1	400	90	20	-	SOIC16	10.4	9.2	96	2.1
SMJ1360	60	250	500	7.000	1	400	26	8	-	SOIC16	10.4	9.2	96	2.1
SMJ1609	100	750	1500	0.500	1	300	75	18	12	DFN12	8	7	56	3
SMJ1619	200	550	1100	1.300	1	300	85	20	12	DFN12	8	7	56	3
SMJ1629	250	450	900	3.500	1	300	70	18	10	DFN12	8	7	56	3
SMJ1659	60	1000	2000	0.175	1	300	90	20	-	DFN12	8	7	56	3
SMJ1660	60	250	500	7.000	1	300	26	8	-	DFN12	8	7	56	3
SMJ1209	100	750	1500	0.500	1	300	75	18	12	DFN12	8	6	48	3
SMJ1259	60	1000	2000	0.175	1	300	90	20	-	DFN12	8	6	48	3
SMJ1260	60	250	500	7.000	1	300	26	8	-	DFN12	8	6	48	3

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Package Marking



Ordering Information

Part Number	Description
SMJ1209	12DFN (Tube packaging)
SMJ1209-TR	12DFN (TNR packaging)

NOTE: Suffixes above are for ordering only and do not appear as device marking

Package Weights

Device	Single Unit
SMJ1209	0.37
SMJ1209-TR	0.37

Note: All weights above are in GRAMS

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Solid State Optronics classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, IPC/JEDEC J-STD-020, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below. Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability. This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard IPC/JEDEC J-STD-033.

Device	MSL Classification
SMJ1209	3

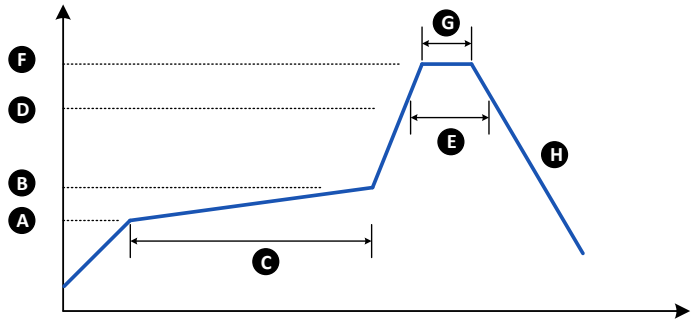
ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard JESD-625.

Solder Profile

1) Infrared Reflow

Refer to the following figure as an example of an optimal temperature profile for single occurrence infrared reflow. Soldering process should not exceed temperature or time limits expressed herein. Surface temperature of device package should not exceed 250°C:



2) Wave Solder:

Not recommended

3) Hand Solder:

Not recommended

Process Step	Description	Parameter
A	Preheat Start Temperature (ºC)	150°C
B	Preheat Finish Temperature (ºC)	180°C
C	Preheat Time (s)	90 - 120s
D	Melting Temperature (ºC)	230°C
E	Time above Melting Temperature (s)	30s
F	Peak Temperature, at Terminal (ºC)	260°C
G	Dwell Time at Peak Temperature (s)	10s
H	Cool-down (ºC/s)	<6°C/s

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